

An Amorphous Silicon Photo TFT with $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ or HfO_2 Double Layered Insulator for Digital Imaging Applications

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Abstract—This paper focuses on amorphous silicon photo thin-film transistors with double layered insulator using $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ or HfO_2 as candidates for the succession of Si_3N_4 as a traditional insulator in the fabrication of hydrogenated amorphous silicon thin-film transistors. Whether for industry or for research, there is a need to investigate the use of thin gate insulators for these devices to overcome leakage current. Our investigations included direct and transfer characteristics in dark and under illumination, generated photocurrents, external quantum efficiency and responsivity. Performance is evaluated in terms of the dielectric thickness and nature. Improvements in the proposed structures regarding off-current, responsivity and quantum efficiency are achieved via these materials. Comparing with $\text{Si}_3\text{N}_4/\text{HfO}_2$ transistor, the $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ device shows the lowest off-current. The HfO_2 device presents the highest on-current when illuminated. The generated photocurrent is higher for $\text{Si}_3\text{N}_4/\text{HfO}_2$ transistor revealing a lower amount of trapped charge. Under illumination and for very thin thicknesses, both devices enhance the Si_3N_4 device off-current and reach Si_3N_4 single layer dielectric based phototransistor performance. external quantum efficiency and responsivity are higher in HfO_2 devices comparing with Al_2O_3 devices. The results are promising and may support further investigations in order to develop high k gate insulators for MIS photo thin-film transistors.

Index Terms—a-Si:H TFT, Al_2O_3 , External Quantum Efficiency, HfO_2 , Photocurrent, Responsivity, Si_3N_4 .

I. INTRODUCTION

Amorphous silicon thin film transistor (a-Si:H TFT) technology is receiving more consideration due its wider applications. The utilization of amorphous silicon TFT is dictated by some advantages like simple fabrication process, high charge transfer rate, low capacitance, high photo-sensitivity and low noise [1]-[3]. In digital radiography, this technology allowed the at panel detectors (FPDs) to be commercially available for many kinds of medical imaging detectors. One way that digital X-ray imaging detectors exploit in detection operation is indirect method. This method consists of the use of a scintillation film that first converts X-rays to visible light, before the electronic signal is obtained by an array of photo-detectors. The elementary building block of FPDs is the pixel which is composed of three components: a sensor for signal acquisition, a storage capacitor for data storage, and a switch for

signal readout [4], [5]. As light sensing element, either phototransistors or photodiodes are used. Comparing with the photodiodes, and despite their slow response time, photo-transistors are preferable because they offer a high optical gain and are compatible with the standard a-Si:H TFTs technology [6], [7]. Since several years and for many applications, many structures for transistors and phototransistors were investigated in order to improve device performance [7]-[14]. Among these structures, were reported transistors with dual layer gate dielectric [15], [16], and/or high k materials as gate dielectrics [17]-[19]. It has been demonstrated that dual-layer dielectric structures are used because of two major advantages: high yield and improved transistors characteristics [20].

In this paper, an amorphous silicon photo TFT (APT) with Si₃N₄/Al₂O₃ or HfO₂ double layered insulator for digital imaging applications is investigated in order to optimize detectors characteristics. The addition of the second dielectric layer is considered while keeping Si₃N₄ for its good interface with amorphous silicon. In an attempt to replace the traditional use of Si₃N₄ (dielectric constant of 6-8), higher k Al₂O₃ (dielectric constant of 8-9) and HfO₂ (dielectric constant of 25) dielectrics are used with this insulator to study APT performance for process integration and size scaling. In fact, Si₃N₄ insulator suffers from its limited capacitance density because of low dielectric constant [16]. As a consequence, there is a limit in the use of thin dielectric layers. A comparative study for three APTs; with Si₃N₄ single dielectric layer (APT1), Si₃N₄/Al₂O₃ double dielectric layer (APT2), then Si₃N₄/HfO₂ double dielectric layer (APT3) structures is done regarding to detectors performance. It is worth noting that our APTs have an aluminum metal gate material. This will contribute in eliminating the depletion capacitance of the gate electrode [18]. Investigations include APTs direct and transfer current characteristics, photocurrent, external quantum efficiency EQE and responsivity R. A comparison between the APTs performance in terms of dielectric nature and thickness is established. The paper is organized as follows: Section II describes the adopted APTs structures, Section III illustrates the obtained results, while Section IV concludes the paper.

II. DEVICE STRUCTURE

The simulations performed in this work were carried out by Silvaco software, it has two modules, Atlas for device simulations and Athena for process simulations. The device structure adopted in this paper is an amorphous silicon based inverted-staggered bottom gate phototransistor. The inverted-staggered bottom gate structure has better characteristics than the top gate (normal or staggered) one [20], [21]. Compared with the normal, staggered transistor, the inverted, staggered TFT has higher field effect mobility μ_{eff} , lower threshold voltage V_{th} , higher on-current I_{on} and lower threshold shift ΔV_{th} under stress [20], [21]. The total structure length and width are 14 μm and 100 μm , respectively. The drain and source contacts lengths are 2 μm each and the channel length is 10 μm . The thicknesses of the undoped and the n+ doped contact a-Si: H layers are 300 nm and 100 nm, respectively. An adequate choice of the a-Si layer thickness was necessary in order to guarantee a layer channel thick enough to maximize the number of absorbed photons on one hand [22], and reduce the contact

resistance on the other hand [6]. In Atlas, the material parameter which defines properties of amorphous silicon is the density of defect states (DOS) [23]. In this tool, the latter is composed of four bands: two tail bands and two deep level ones. The tail bands are composed of a donor-like valence band and an acceptor-like conduction band. The deep bands are composed of one acceptor-like band and one donor-like band. These are modeled using a Gaussian distribution as follows [23]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (1)$$

Where E is the trap energy and the subscripts T, G, A and D denote respectively tail, Gaussian, acceptor and donor states. g_{TA} , g_{TD} , g_{GA} and g_{GD} are expressed by [23]:

$$g_{TA}(E) = NTA \exp\left(\frac{E-E_C}{WTA}\right) \quad (2)$$

$$g_{TD}(E) = NTD \exp\left(\frac{E_V-E}{WTD}\right) \quad (3)$$

$$g_{GA}(E) = NGA \exp\left[-\left(\frac{E_{GA}-E}{WGA}\right)^2\right] \quad (4)$$

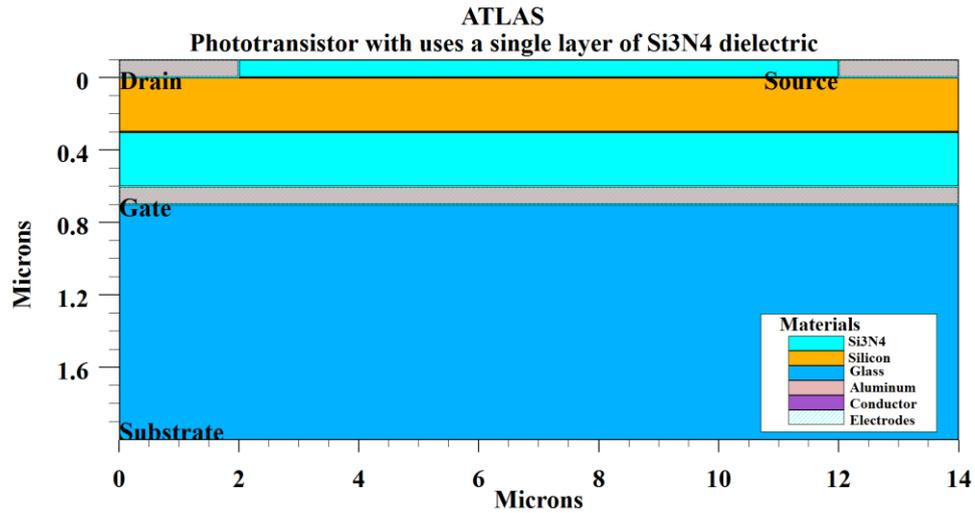
$$g_{GD}(E) = NGD \exp\left[-\left(\frac{E-E_{GD}}{WGD}\right)^2\right] \quad (5)$$

E_C is the conduction band edge energy and E_V is the valence band edge energy. The DOS parameters can be specified by the user. Table I shows the user-specifiable parameters for the density of defect states [24]. In this table, for the exponential tail distribution NTA and NTD are the conduction and valence band edge intercept densities, WTA and WTD are the DOS characteristic decay energies. For the Gaussian distribution, NGA and NGD are densities for acceptor-like donor-like bands, respectively, and EGA and EGD are peaks for energy distribution [23].

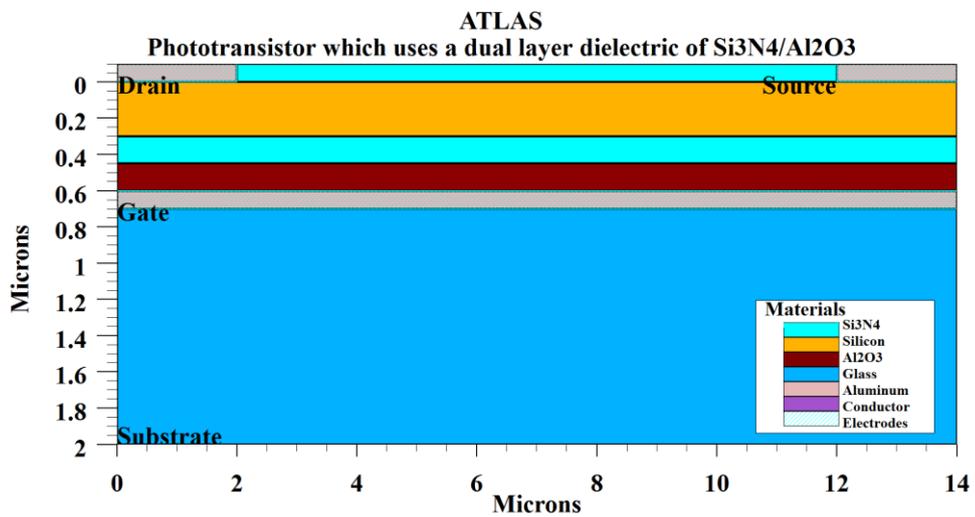
TABLE I: USER-SPECIFIABLE PARAMETERS FOR THE DENSITY OF DEFECT STATES [23], [24]

Parameter	Value	Units
NTA	1×10^{21}	cm^{-3}/eV
NTD	1×10^{21}	cm^{-3}/eV
NGA	1×10^{16}	cm^{-3}/eV
NGD	1×10^{16}	cm^{-3}/eV
EGA	0.6	eV
EGD	0.6	eV
WTA	0.05	eV
WTD	0.05	eV
WGA	0.3	eV
WGD	0.3	eV
EG	1.8	eV

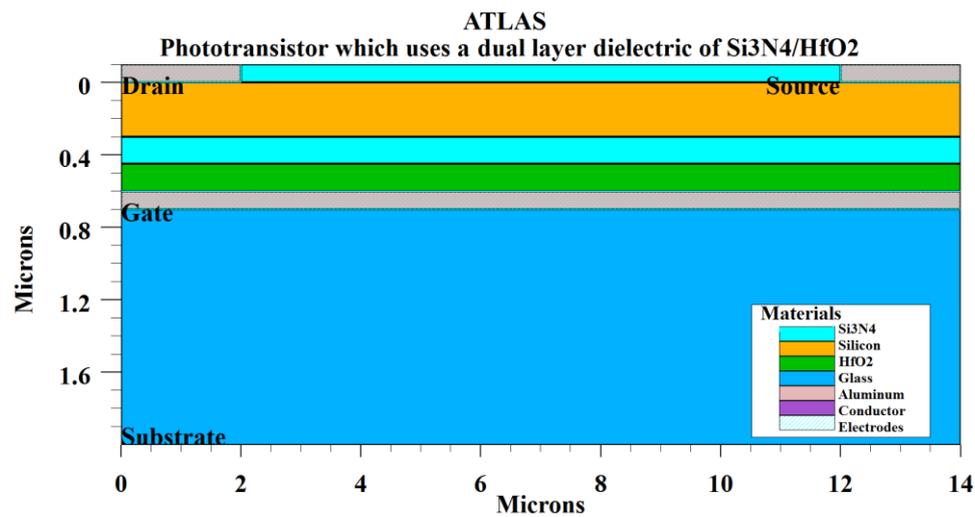
Various physical and mathematical models have been used to perform analysis in Atlas: Shockley-Read Hall (SRH) model and physical models for recombination mechanisms and carrier mobility, and Newton and Gummel method for numerical simulations. Cross sections of the adopted transistor structures for our simulations are illustrated on . Fig. 1a shows a phototransistor with a single layer of a Si_3N_4 dielectric, Fig. 1b shows the photo-transistor which uses a dual layer dielectric of $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$, and Fig. 1c shows a phototransistor which uses a dual layer dielectric of $\text{Si}_3\text{N}_4/\text{HfO}_2$.



(a)



(b)



(c)

Fig. 1. The APTs under study: (a) APT1, (b) APT2 and (c) APT3.

III. RESULTS AND DISCUSSION

A. Wavelength Selectivity

In indirect pixels, phototransistors, as sensing devices, are designed to detect visible light. The fact that absorption of visible light is more important in amorphous silicon than in crystalline silicon [25] will help to reduce optical loss and improve photoelectric conversion efficiency [25]. To probe the wavelength selectivity of our APTs, the drain current was simulated under visible light with a gate-to-source voltage VGS and a drain-to-source voltage VDS equal to 10 V and 0.1 V respectively. The results are shown on Fig. 2. This figure shows clearly a higher sensitivity in the blue region.

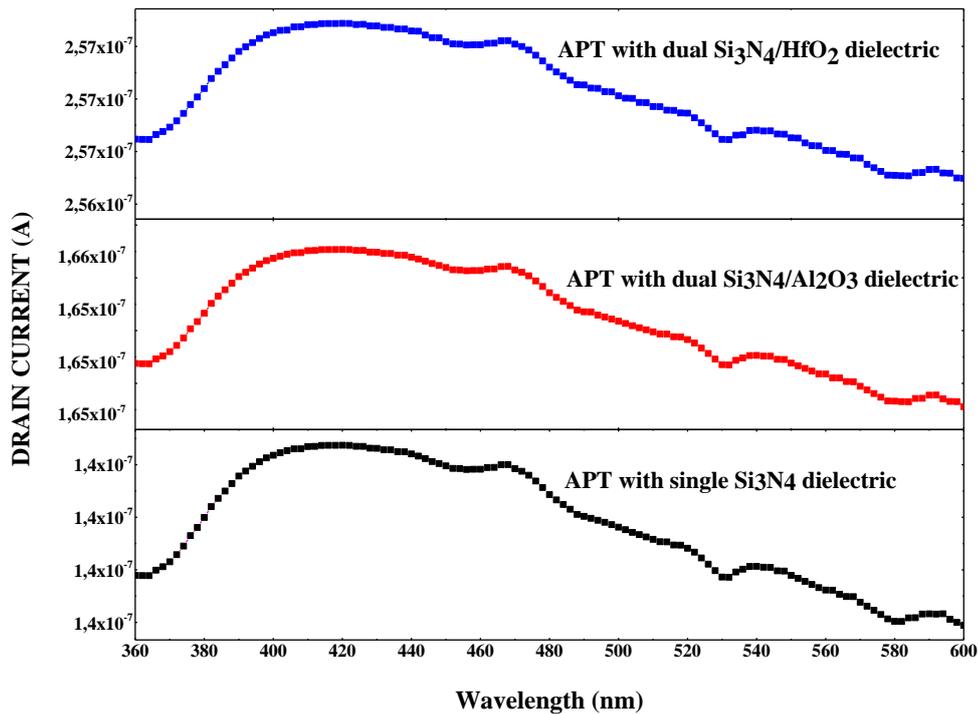


Fig. 2. Wavelength selectivity of the APTs under study.

The drain current peaks at a wavelength of 420 nm for the three APTs where most of the light intensity was absorbed by the 300 nm a-Si layer. The peak is situated around 0.14 A for the single layer dielectric APT, 0.17 A for the $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ dual layer dielectric APT, and 0.26 A for the $\text{Si}_3\text{N}_4/\text{HfO}_2$ dual layer dielectric APT. Below this wavelength, absorption in the amorphous silicon layer increases, while beyond, recombination at the a-Si/insulator interface dominates. This response matches well with that found in [7], [26]. This result suggests the use of a Lutetium Oxyorthosilicate (Ce) scintillator or a Sodium doped Cesium Iodide (CsI:Na) scintillator whose emission spectra peak matches well with absorption peak spectral of our APTs for an optimum of performance [22], [27]. On the other hand, to reinforce the above mentioned result, the photogeneration rate of our phototransistors was simulated by illumination of the devices from the top side with 0.16 mW/cm² light intensity, and 365 nm, 420 nm and 550 nm wavelengths. The results are shown on Fig. 3. The latter reveals again that the photogeneration rate is the highest for the wavelength of 420 nm.

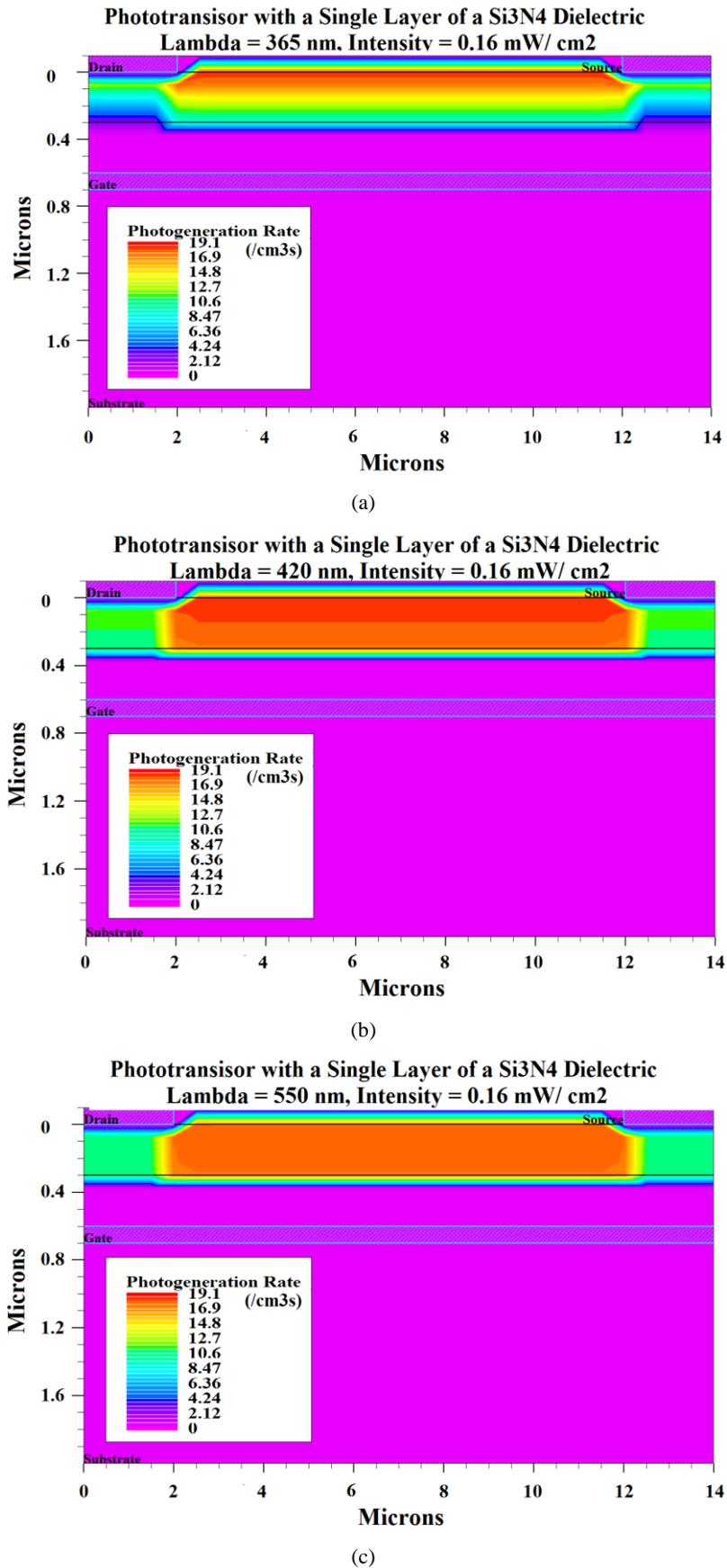


Fig. 3. Photogeneration rate in the phototransistor with (Si₃N₄) gate dielectric for (a) 365 nm, (b) 420 nm and (c) 550 nm wavelengths under 0.16 mW/cm².

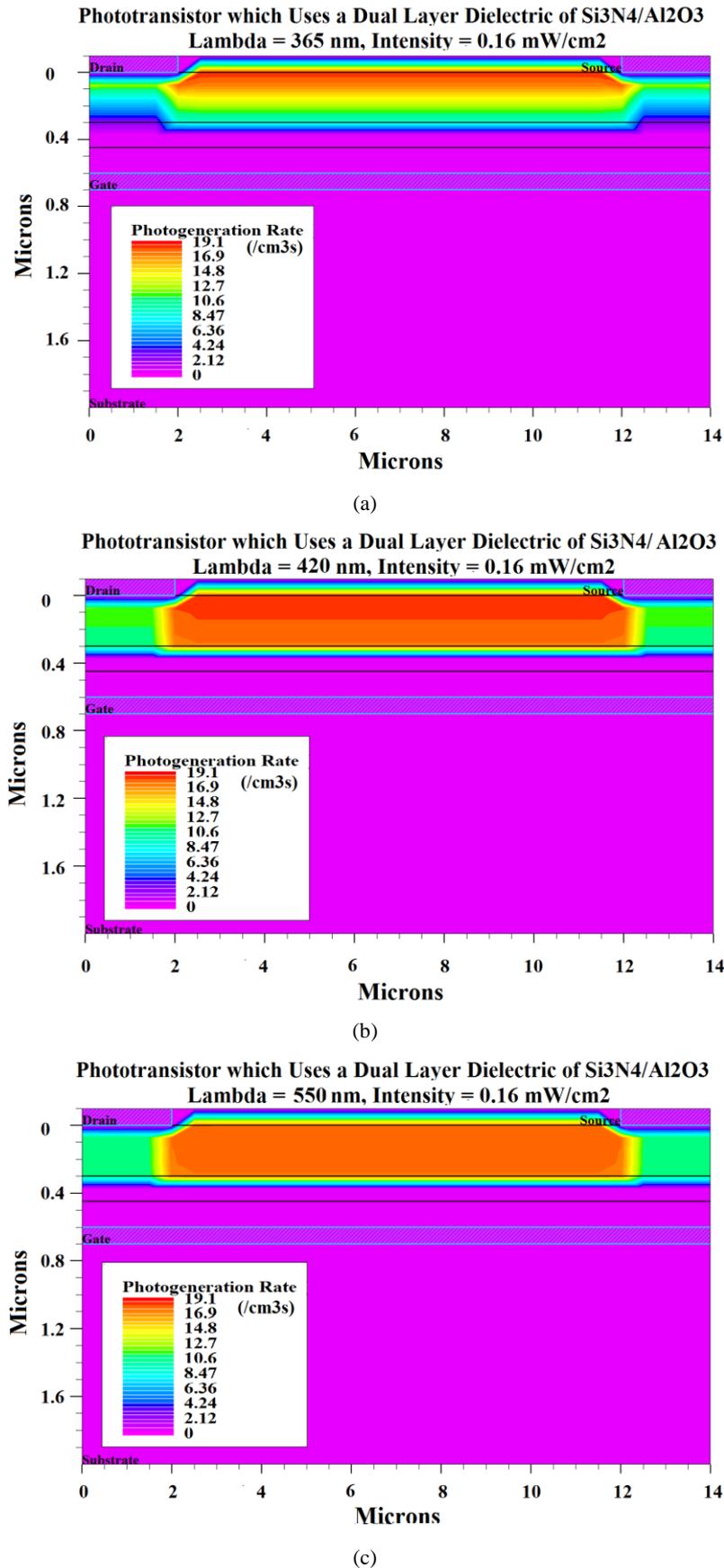


Fig. 4. Photogeneration rate in the phototransistor with (Si₃N₄/Al₂O₃) gate dielectric for (a) 365 nm, (b) 420 nm and (c) 550 nm wavelengths under 0.16 mW/cm².

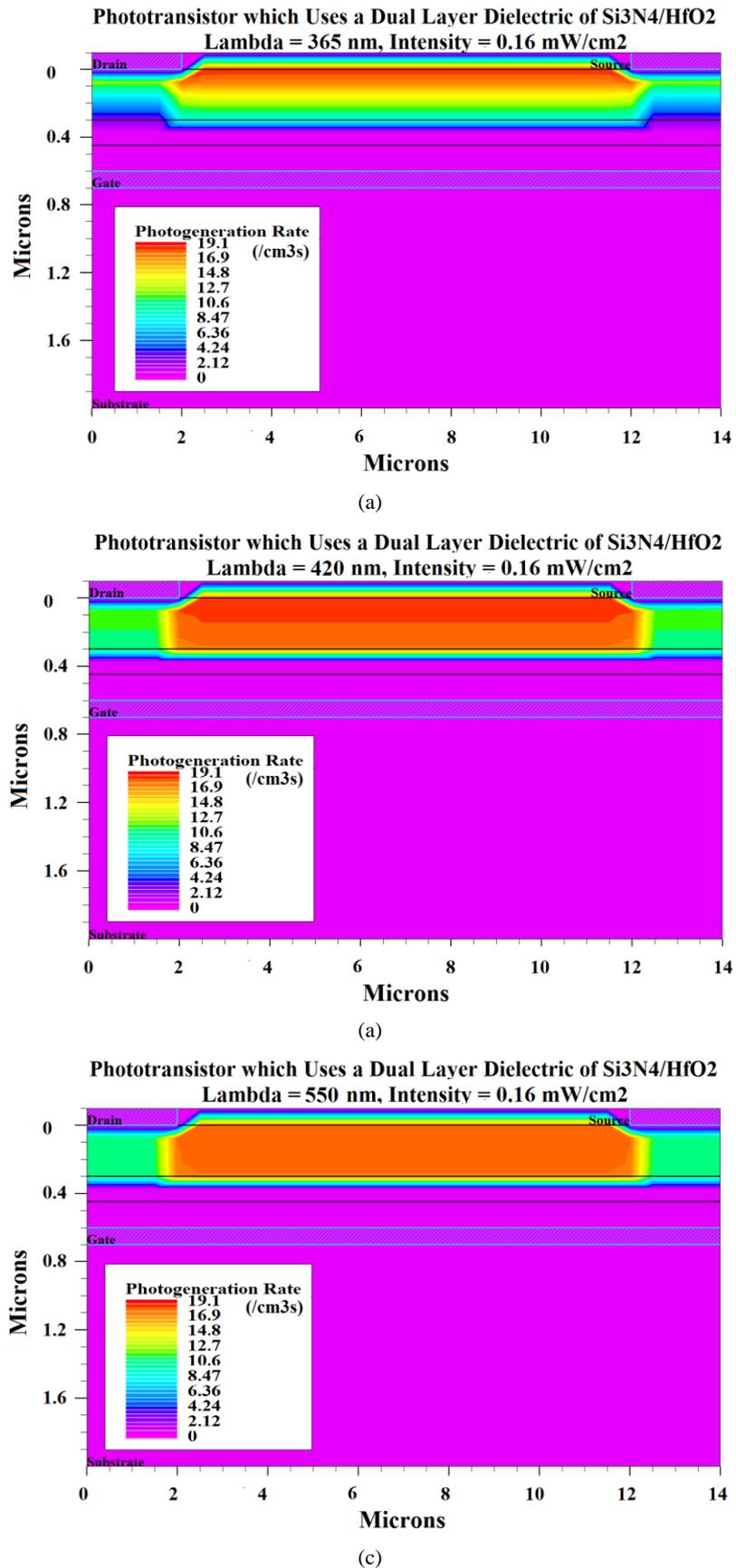


Fig. 5. Photogeneration rate in the phototransistor with (Si₃N₄/HfO₂) for (a) 365 nm, (b) 420 nm and (c) 550 nm wavelengths under 0.16 mW/cm².

B. Current-Voltage Characteristics in Dark and Under Illumination

Taken as a reference, the amorphous phototransistor APT1 with Si₃N₄ single dielectric layer was first investigated. Under light intensity of 0.16 mW/cm² and using a wavelength of 420 nm, dark and illumination characteristics of the device were simulated. Transfer and direct characteristics are illustrated on Fig. 6. This figure illustrates the obtained results for Si₃N₄ thicknesses of 1 nm, 30 nm, and 150 nm. Threshold voltage, on- and off- currents for these figures are given on Table II.

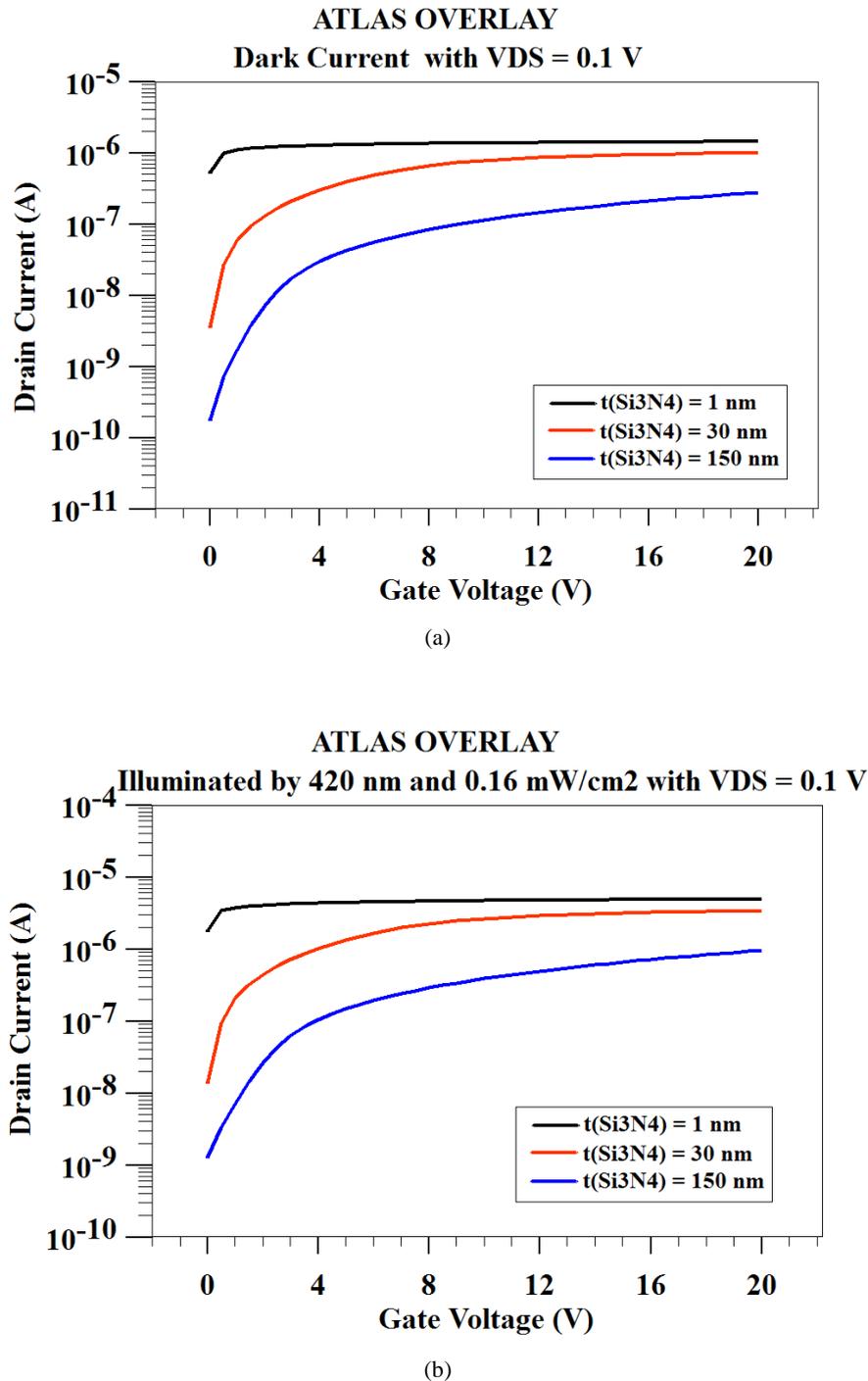


Fig. 6. Transfer characteristics of APT1. (a) in dark, (b) under illumination with 420 nm.

TABLE II: THRESHOLD VOLTAGE, ON- AND OFF-CURRENTS FOR FIG. 6 .

	Vt		Ion		Ioff	
	Dark	Light	Dark	Light	Dark	Light
Si ₃ N ₄ = 1 nm	0.6	0.61	1.43×10 ⁻⁶	4.93×10 ⁻⁶	5.23×10 ⁻⁷	1.78×10 ⁻⁶
Si ₃ N ₄ = 30 nm	0.9	0.89	1.00×10 ⁻⁶	3.41×10 ⁻⁶	3.66×10 ⁻⁹	1.39×10 ⁻⁸
Si ₃ N ₄ =150 nm	4.6	4.56	2.80×10 ⁻⁷	9.54×10 ⁻⁷	1.79×10 ⁻¹⁰	1.30×10 ⁻⁹

In dark condition, the drain current is significant when Si₃N₄ layer is very thin. When the latter becomes thicker, it decreases and the leakage becomes weaker. Under illumination (Fig. 6b), the current rises significantly revealing a high generation of electron-hole pairs. The off-current is the lowest and the threshold voltage is higher for 150 nm insulator thickness. However, the on-current is higher for 1nm not with a big difference with 30 nm insulator thickness. Thus, regarding off-current, illumination on-current, and threshold voltage findings, a trade-off was made to take an Si₃N₄ thickness of 30 nm.

Under the same conditions as for APT1, a comparative study for the three APTs with Si₃N₄ single dielectric layer (APT1), as a reference, Si₃N₄/Al₂O₃ double dielectric layer (APT2), and Si₃N₄/HfO₂ double dielectric layer (APT3) structures is done regarding to the nature of the used dielectric and its thickness. Fig. 7 - Fig. 9 show in dark transistors direct and transfer characteristics for Al₂O₃ and HfO₂ thicknesses of 1 nm, 30 nm and 150 nm, while maintaining Si₃N₄ thickness equal to 30 nm. For 1 nm thickness (Fig. 7), even dark currents are comparable for the three structures, the one with Si₃N₄/Al₂O₃ has the lowest dark current. Al₂O₃ and HfO₂ are very thin enabling leaks to happen. The threshold voltages are also comparable. They are of 0.93 V for Si₃N₄/Al₂O₃ combination and of 0.91 V for Si₃N₄/HfO₂ combination. The dark off-currents are in the order of 3 nA. Fig. 8 shows that for 30 nm /30 nm, the amount of dark current is lower when Al₂O₃ is used with Si₃N₄.

The off-current is approximately equal to 1.07 nA for Al₂O₃ while it reaches 1.91 nA approximately for HfO₂ as a second dielectric. The threshold voltage varies from 1.9 V with Al₂O₃ to 1.3 V with HfO₂ When the insulator second layer is thicker (150 nm), regarding Fig. 9, Si₃N₄/Al₂O₃ presents the lowest dark current. The off-current varies from 0.177 nA for Si₃N₄/Al₂O₃ to 0.526 nA for Si₃N₄/HfO₂. The threshold voltage varies from 4.6 V for the former to 3 V for the latter. Thus as a preliminary conclusion, one can conclude that use of Al₂O₃ and HfO₂ combined with Si₃N₄ as gate insulators for APTs reduces the dark current which may enhance the dynamic range of photodetectors [11]. As for under dark conditions, our transistors responses were analyzed under illumination for the same conditions.

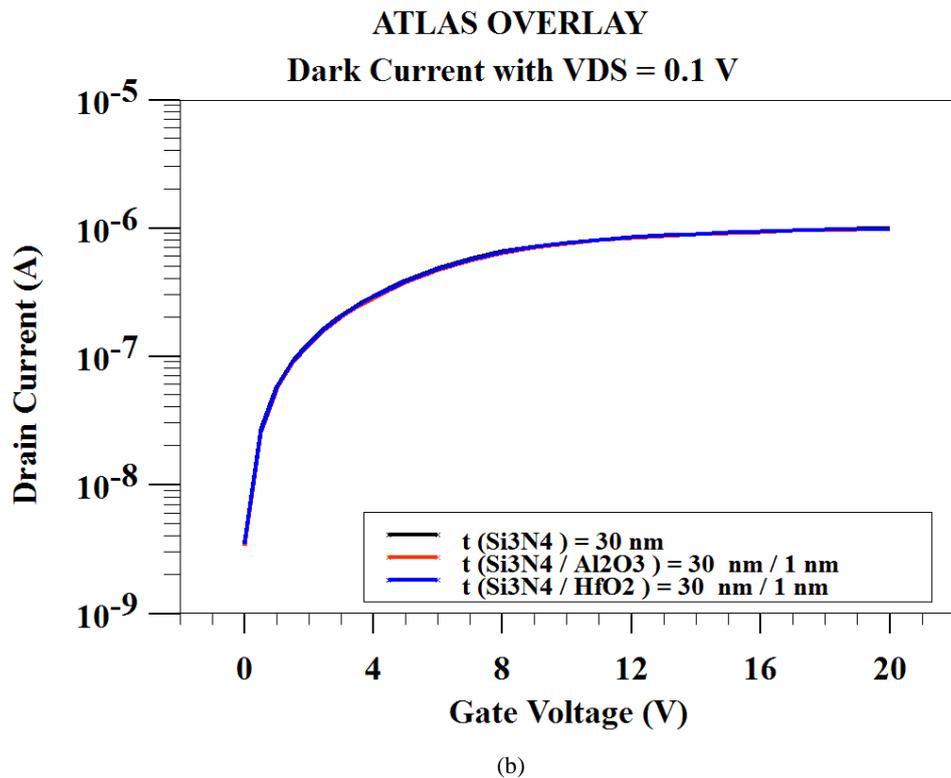
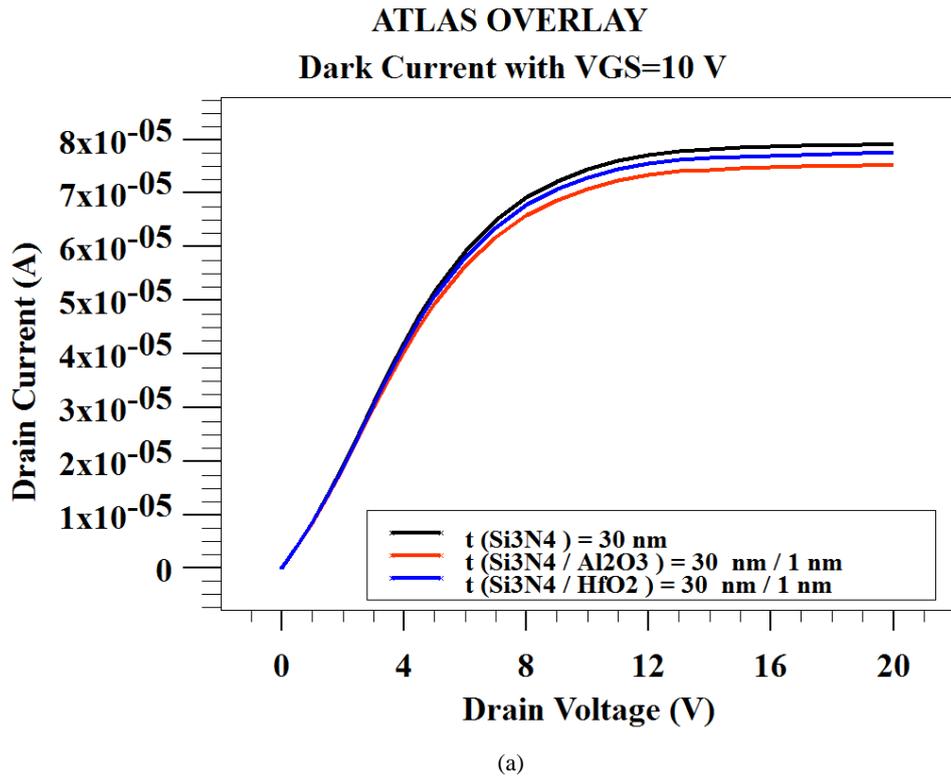


Fig. 7. (a) Direct and (b) transfer characteristics of the APTs under study for 1nm second dielectric layer thickness in dark.

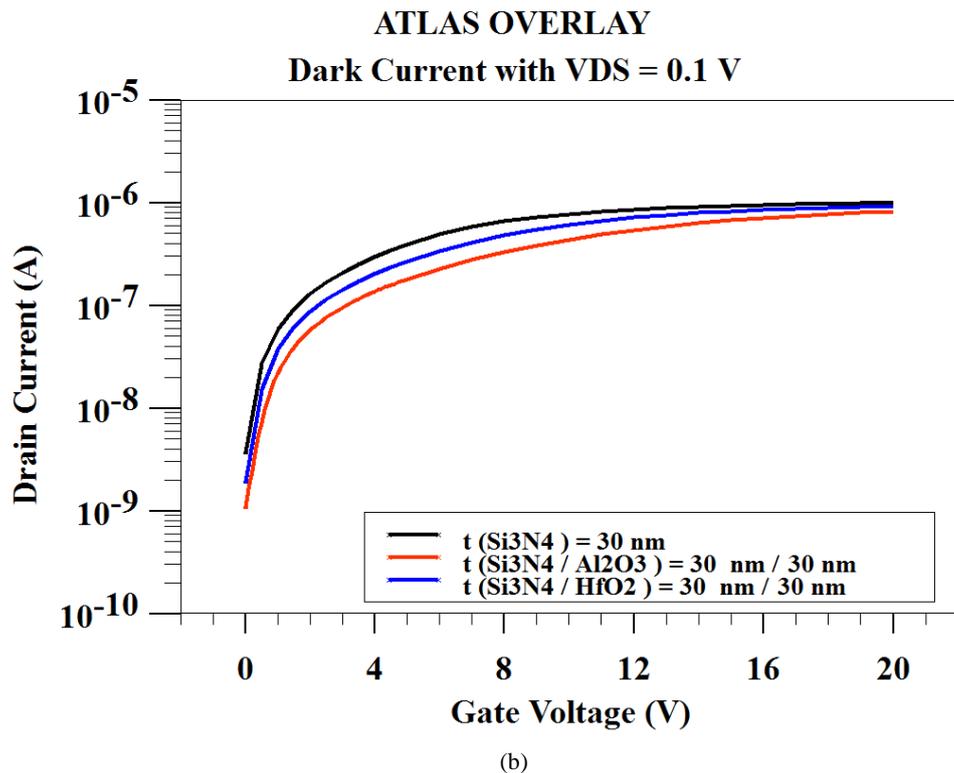
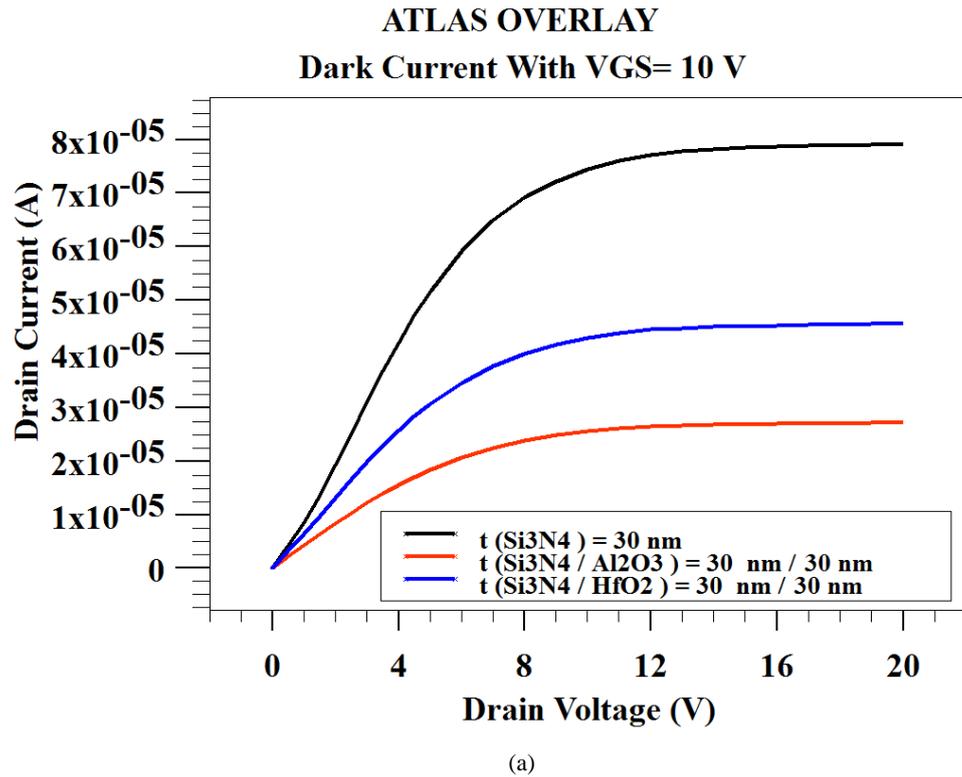


Fig. 8. (a) Direct and (b) transfer characteristics of the APTs under study for 30 nm second dielectric layer thickness in dark.

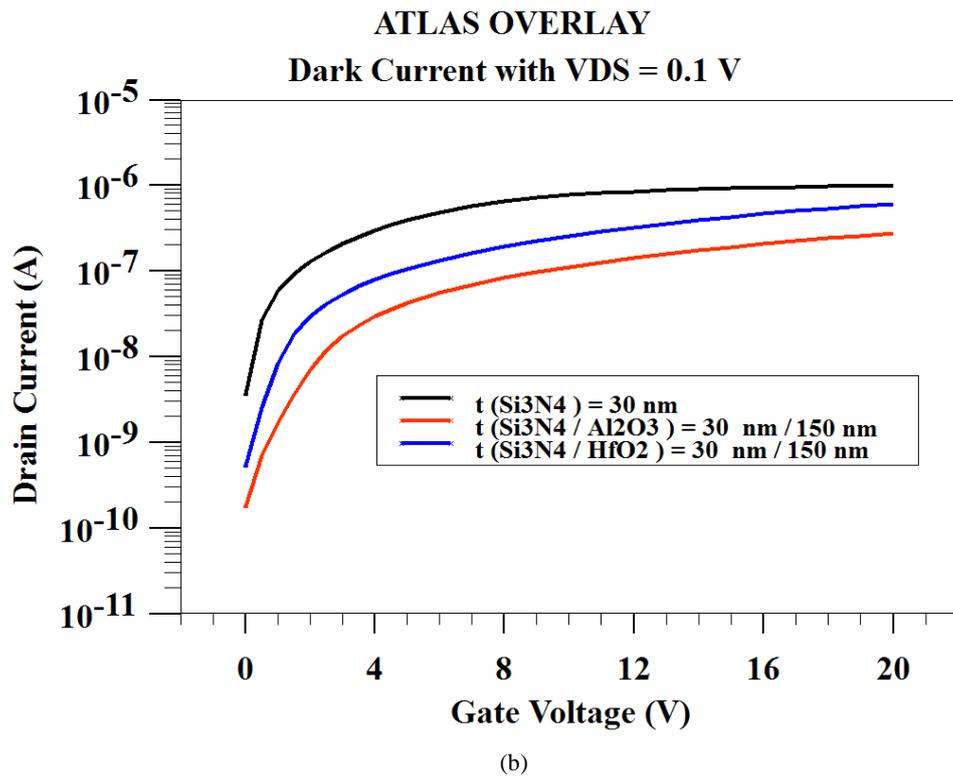
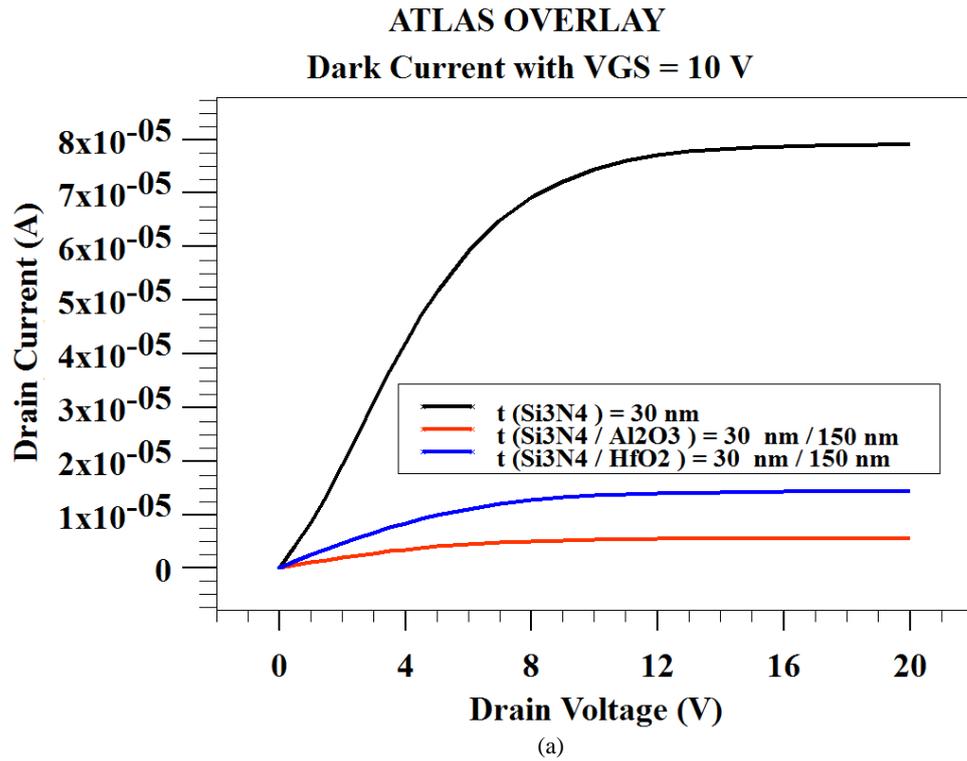


Fig.9. (a) Direct and (b) transfer characteristics of the APTs under study for 150 nm second dielectric layer thickness in dark.

Fig. 10 - Fig. 12 show the obtained results for both direct and transfer characteristics. In accordance with Fig. 10, for 1 nm thickness of Al₂O₃ combined with Si₃N₄, the results show once again expected comparables results for the three APTs in terms of current and threshold voltage. From 30 nm to 31 nm the difference is not noticeable although the photogeneration effect.

Table III gives the obtained values for on- and off-currents, and threshold voltages. The on-to-off current ratio is 2.52×10^2 for APT3 and is 2.6×10^2 for APT2 when Al₂O₃ is used. For 30 nm thickness of Al₂O₃ and HfO₂, the results show that under illumination by 420 nm wavelength, even the off-current is minimum for APT2 (use of Al₂O₃), the use of HfO₂ as a second insulating layer gives higher on-current. The values are 3.15 μ A for Si₃N₄/HfO₂ combination while they are of 2.79 μ A for Si₃N₄/Al₂O₃ combination. The respective threshold voltages are 1.3 V and 1.9 V approximately. The on-to-off current ratio is 4×10^2 for APT3 and is 6×10^2 for APT2. It is thus higher for APT2 when Al₂O₃ is used with Si₃N₄. For 150 nm thickness of Al₂O₃ and HfO₂, Fig. 12 shows that when enough thick, the use of HfO₂ as a second insulating layer presents the highest on-current under illumination. The values are 2.05 μ A for Si₃N₄/HfO₂ combination and 0.946 μ A for Si₃N₄/Al₂O₃ combination (Table. III), respectively. The respective threshold voltages are 3 V and 4.57 V. Respective On-to-off currents are 7.8×10^2 and 7.28×10^2 . It is worth noting that, if Al₂O₃ in APT2 improves the off-current, the on-current under illumination is higher for HfO₂ in APT3 than for APT2. The same findings were reported in [17] and in [19] where it was shown that the Al₂O₃ transistors show the best subthreshold slope and the interface trap density and that the HfO₂ transistors reach a higher transconductance.

TABLE III: THRESHOLD VOLTAGES, ON- AND OFF- CURRENTS FOR FIG.7- FIG. 12.

	V _t		I _{on}		I _{off}	
	Dark	Light	Dark	Light	Dark	Light
t(Si ₃ N ₄) = 30 nm	0.89	0.88	1.00×10^{-6}	3.41×10^{-6}	3.66×10^{-9}	1.39×10^{-8}
t (Si ₃ N ₄ /Al ₂ O ₃)= 30 nm/1 nm	0.93	0.93	9.94×10^{-7}	3.39×10^{-6}	3.44×10^{-9}	1.31×10^{-8}
t (Si ₃ N ₄ /HfO ₂) = 30 nm/1 nm	0.9	0.9	9.98×10^{-7}	3.40×10^{-6}	3.57×10^{-9}	1.35×10^{-8}
t (Si ₃ N ₄) = 30 nm	0.89	0.88	1.00×10^{-6}	3.41×10^{-6}	3.66×10^{-9}	1.39×10^{-8}
t(Si ₃ N ₄ /Al ₂ O ₃) = 30 nm/30 nm	1.9	1.89	8.18×10^{-7}	2.79×10^{-6}	1.07×10^{-9}	4.61×10^{-9}
t (Si ₃ N ₄ /HfO ₂) = 30 nm/30 nm	1.3	1.3	9.25×10^{-7}	3.15×10^{-6}	1.91×10^{-9}	7.67×10^{-9}
t(Si ₃ N ₄) = 30 nm	0.89	0.88	1.00×10^{-6}	3.41×10^{-6}	3.66×10^{-9}	1.39×10^{-8}
t (Si ₃ N ₄ /Al ₂ O ₃) = 30 nm/150 nm	4.57	4.55	2.70×10^{-7}	9.46×10^{-7}	1.77×10^{-10}	1.30×10^{-9}
t (Si ₃ N ₄ /HfO ₂) = 30 nm/150 nm	3.02	3.01	6.01×10^{-7}	2.05×10^{-6}	5.26×10^{-10}	2.62×10^{-9}

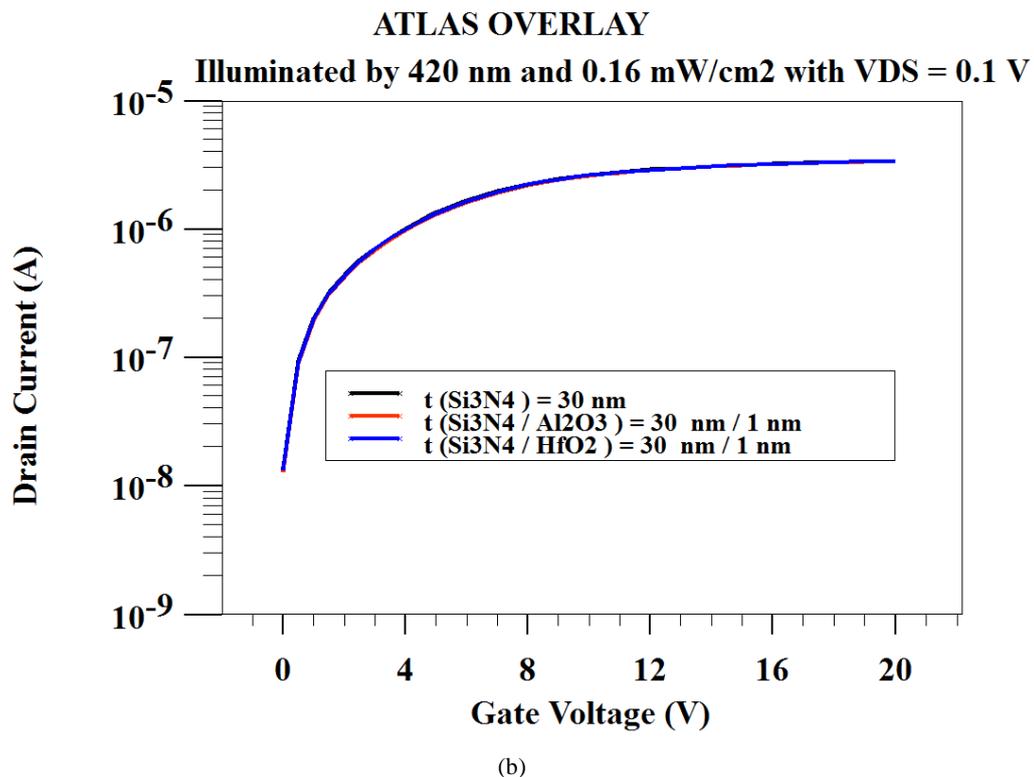
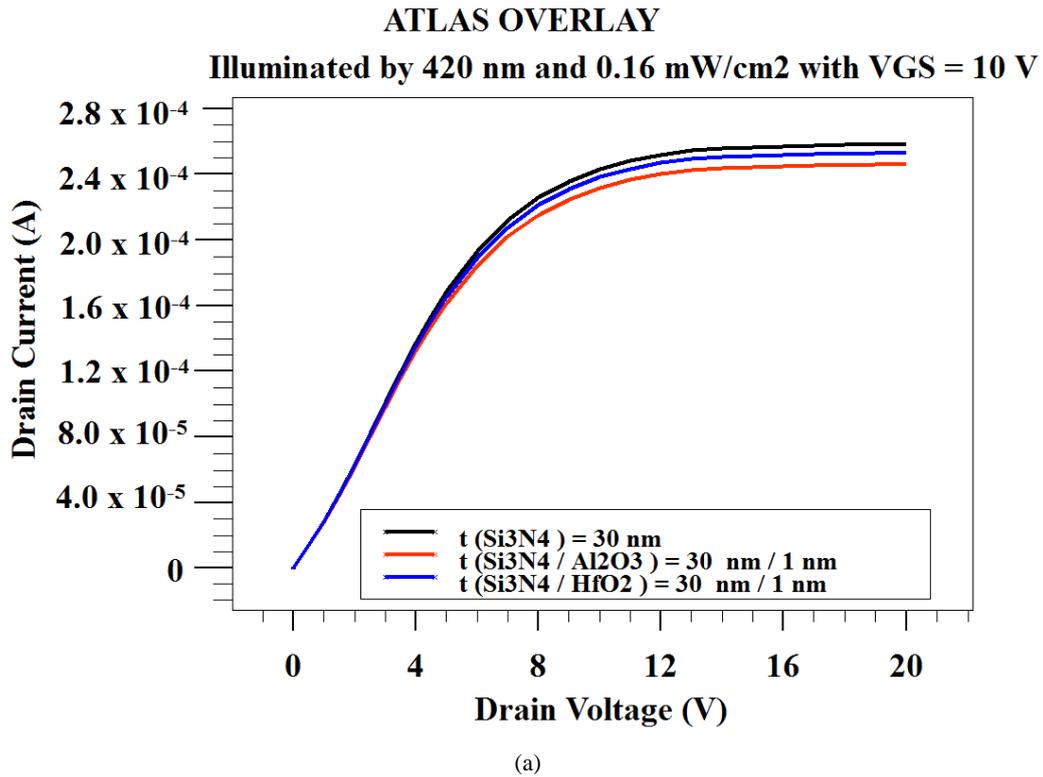


Fig. 10. (a) Direct and (b) transfer characteristics of the APTs under study for 1nm second dielectric layer thickness and under illumination with 420 nm.

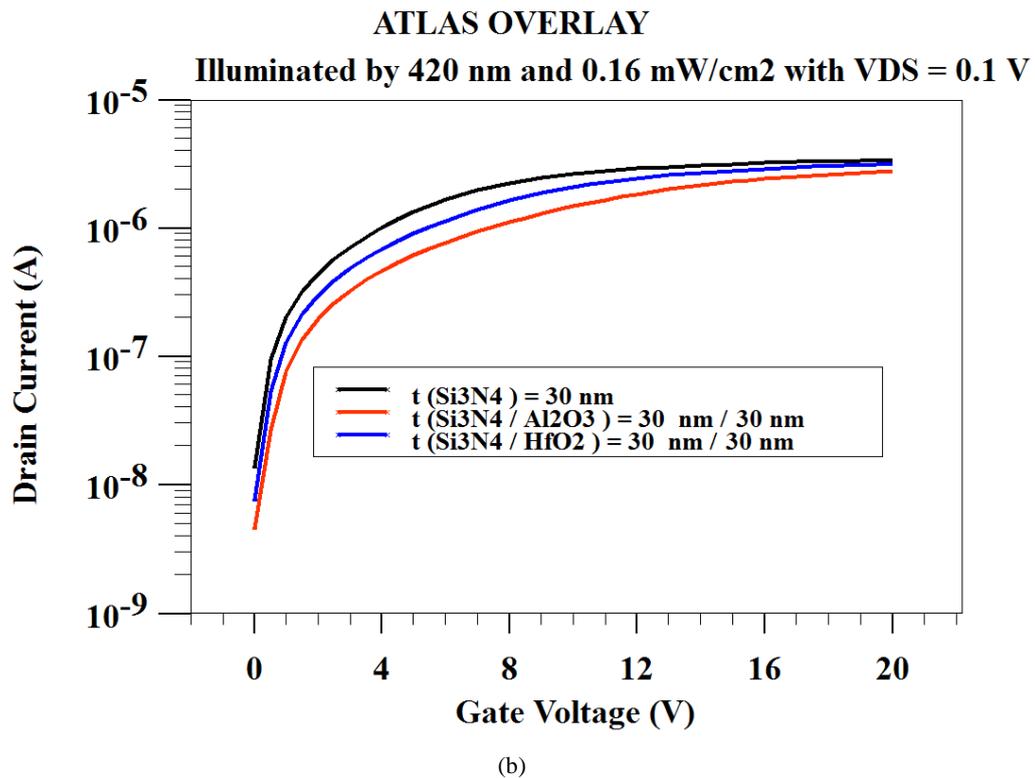
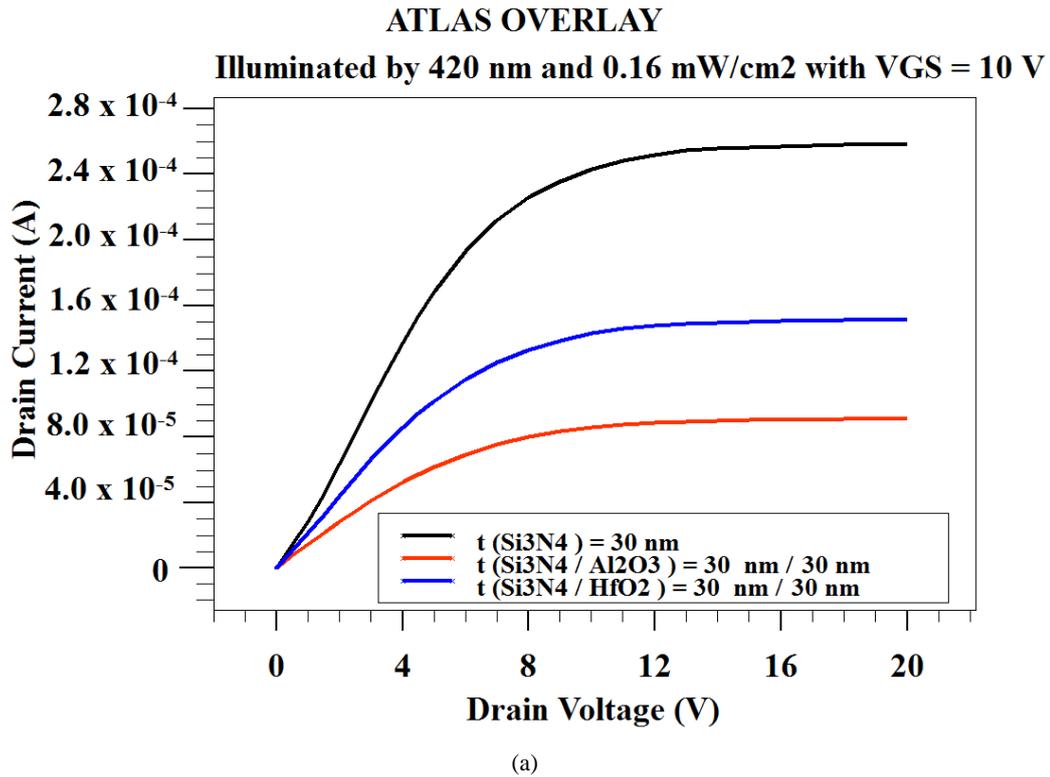


Fig. 11. (a) Direct and (b) transfer characteristics of the APTs under study for 30nm second dielectric layer thickness under illumination with 420 nm.

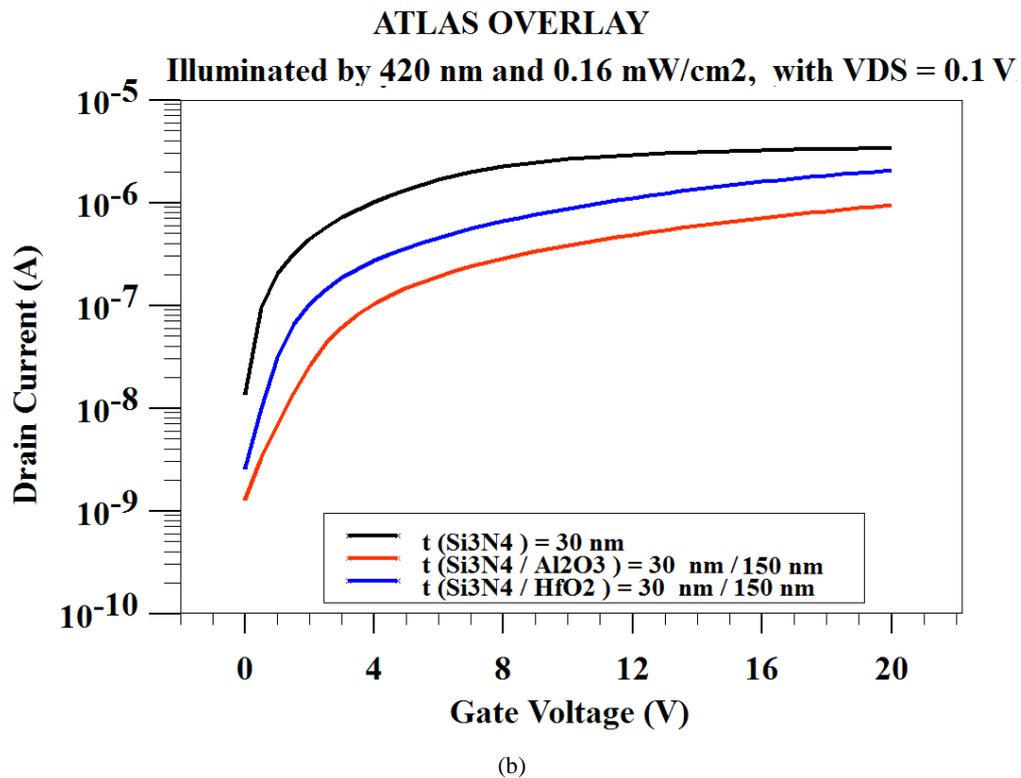
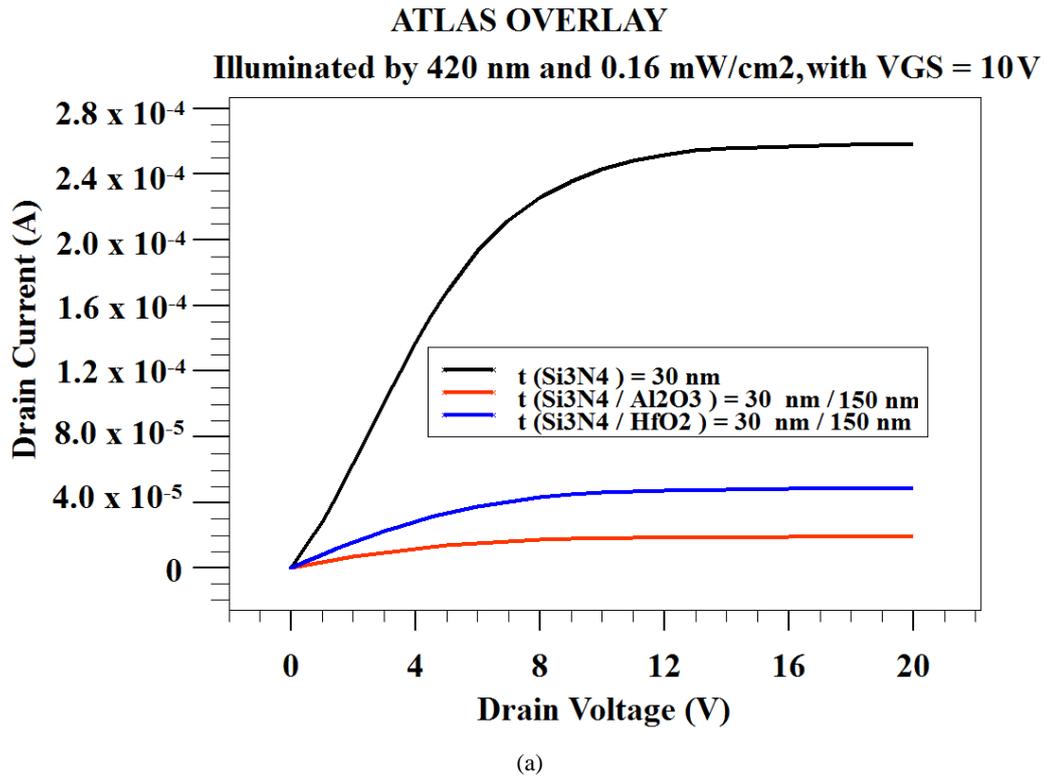


Fig. 12. (a) Direct and (b) transfer characteristics of the APTs under study for 150nm second dielectric layer thickness under illumination with 420 nm.

On the other hand, the resulting photocurrent generated in our three APTs in terms of high k dielectric nature is shown on Fig. 13, and in terms of dielectric thickness on Fig. 14. As mentioned earlier, Fig. 13 reveals that the HfO_2 device has higher photocurrent versus Al_2O_3 device. As a function of the dielectrics thicknesses, Fig. 14 shows that, as expected, thinner insulator thickness generates higher photocurrent and higher leakage current as well. From dark and illumination results all together, one can conclude that comparing with Si_3N_4 device, the leakage property is improved with Al_2O_3 and HfO_2 insulators as was reported in [20] due the high k effect, and further in the Al_2O_3 device for its better off-current characteristics comparing with HfO_2 device. This can be attributed to the very low defect density in $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ system [15], [28]. Under illumination, the on-current for HfO_2 device is higher for all the APTs revealing the drift as the dominant component of photocurrent and /or lower trapping mechanisms [11].

C. External Quantum Efficiency and Responsivity

Our detectors were also investigated in terms of external quantum efficiency EQE, and responsivity R which are effective performance metrics for imaging applications. A detectors EQE indicates if the detector is capable to convert optical signal to electrical signal, while responsivity defines transfer gain. The latter is the ratio of the photocurrent flowing through the detector to the incident optical power. It is given by the expression [29]:

$$R = \frac{(I_{\text{illumination}} - I_{\text{dark}})}{P} = \frac{I_{\text{ph}}}{P} \quad (6)$$

where $I_{\text{illumination}}$ is the total current under illumination, I_{ph} is the photocurrent, I_{dark} is the dark current and P is the power of the incident light per unit area. The EQE is given by the expression [29]:

$$\text{EQE} = \frac{I_{\text{ph}}/q}{P/h\nu} \quad (7)$$

Fig. 15 and Fig. 16 show EQE and responsivity of our phototransistors as a function of the drain voltage for different insulators thicknesses when illuminated with visible blue light at power density of 0.16 mW/cm^2 and biased at $V_{\text{GS}} = 10 \text{ V}$. In Fig. 15, EQEs higher than unity are obtained. As expected, thicker insulators degrade the devices efficiently. APTs with HfO_2 as a second dielectric layer exhibit higher efficiency because of the higher photogenerated current. At 150 nm , gain lower than unity is obtained revealing a decreased number of photogenerated carriers. As illustrated by Fig. 16, the same trends are obtained for responsivity. As expected, in terms of thickness, thinner insulators give higher transfer gains due to higher photocurrents. HfO_2 APT gives better responsivity than Al_2O_3 . Responsivity saturates for high drain voltages following the saturation of the photogenerated current.

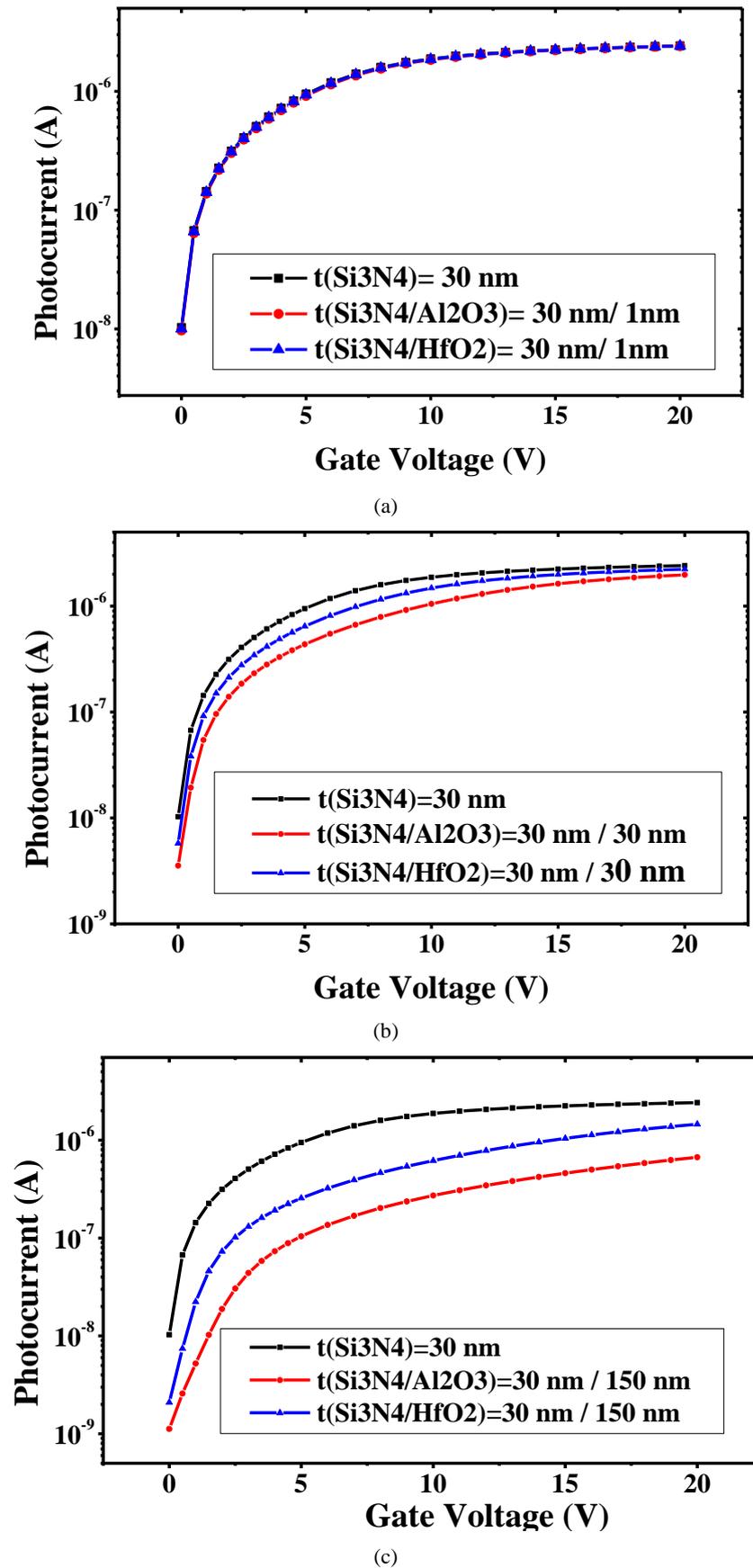
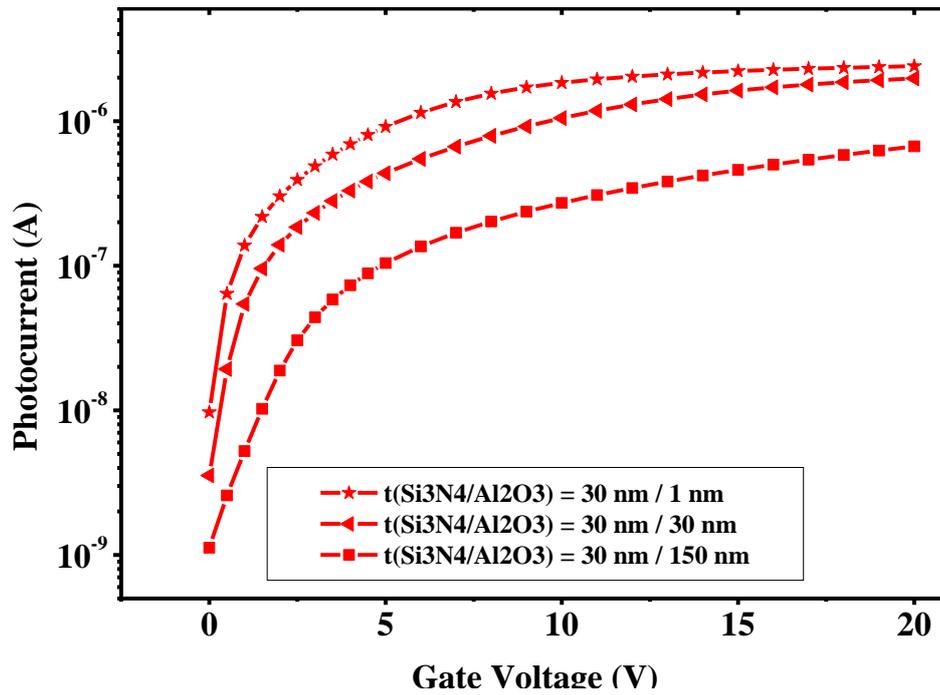
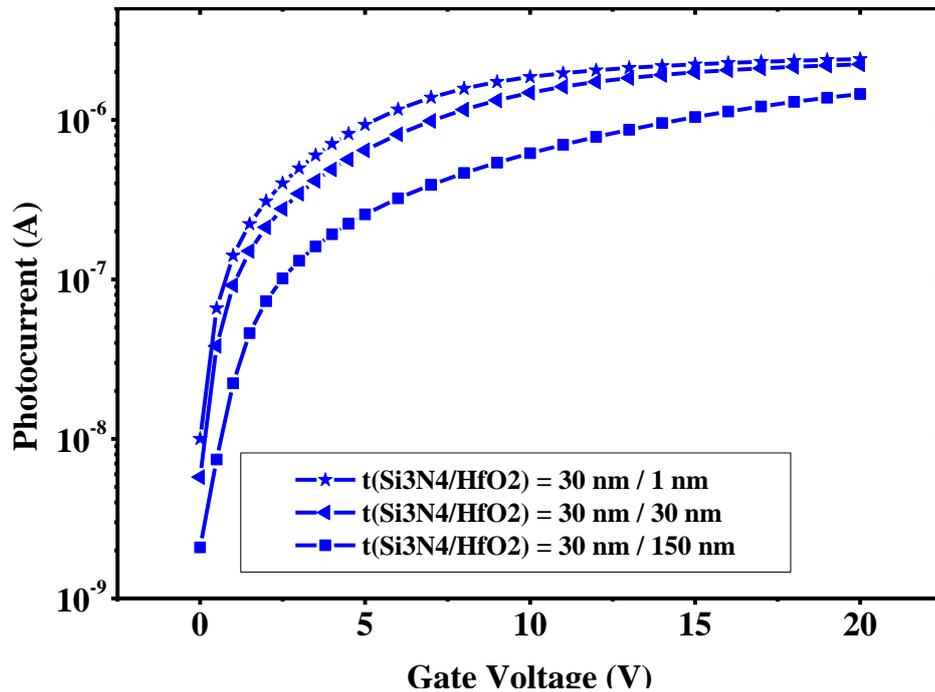


Fig. 13. Generated photocurrent vs gate voltage for the APTs under study illuminated by 420 nm for different second layer dielectric thickness .

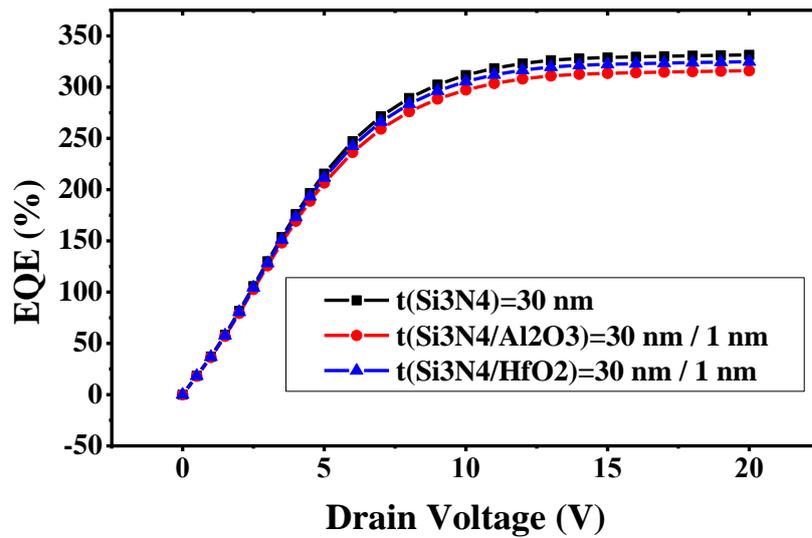


(a)

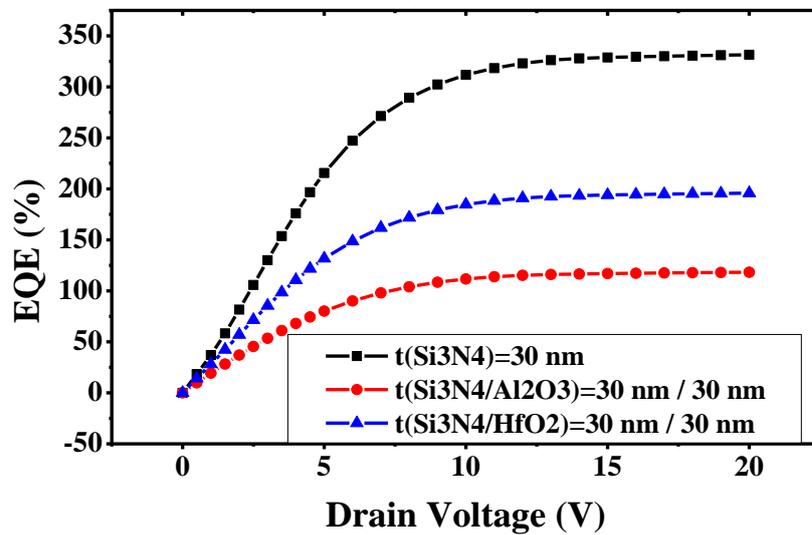


(b)

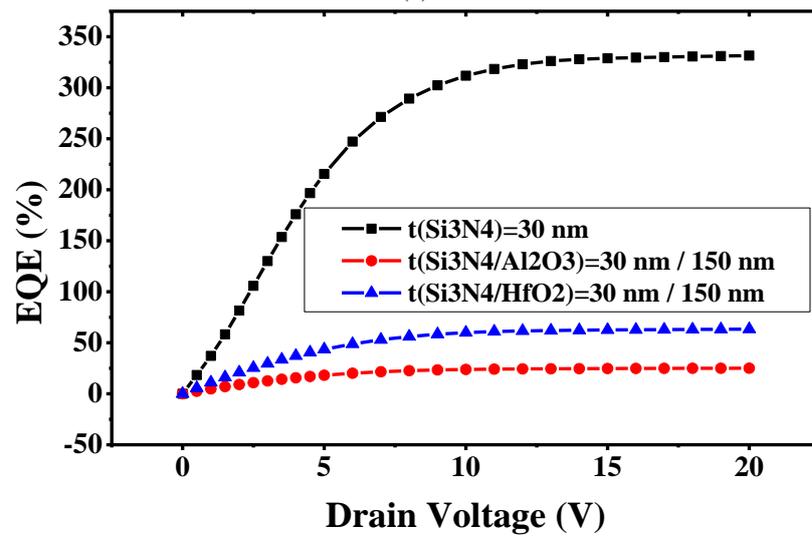
Fig. 14. Generated photocurrent vs gate voltage of APT2 and APT3 illuminated by 420 nm for (a) Si₃N₄/Al₂O₃ combination thickness and (b) Si₃N₄/HfO₂ combination thickness.



(a)



(b)



(c)

Fig. 15. EQE vs drain voltage for the APTs under study illuminated by 420 nm for second dielectric layer thickness of (a) 1 nm, (b) 30 nm and (c) 150 nm.

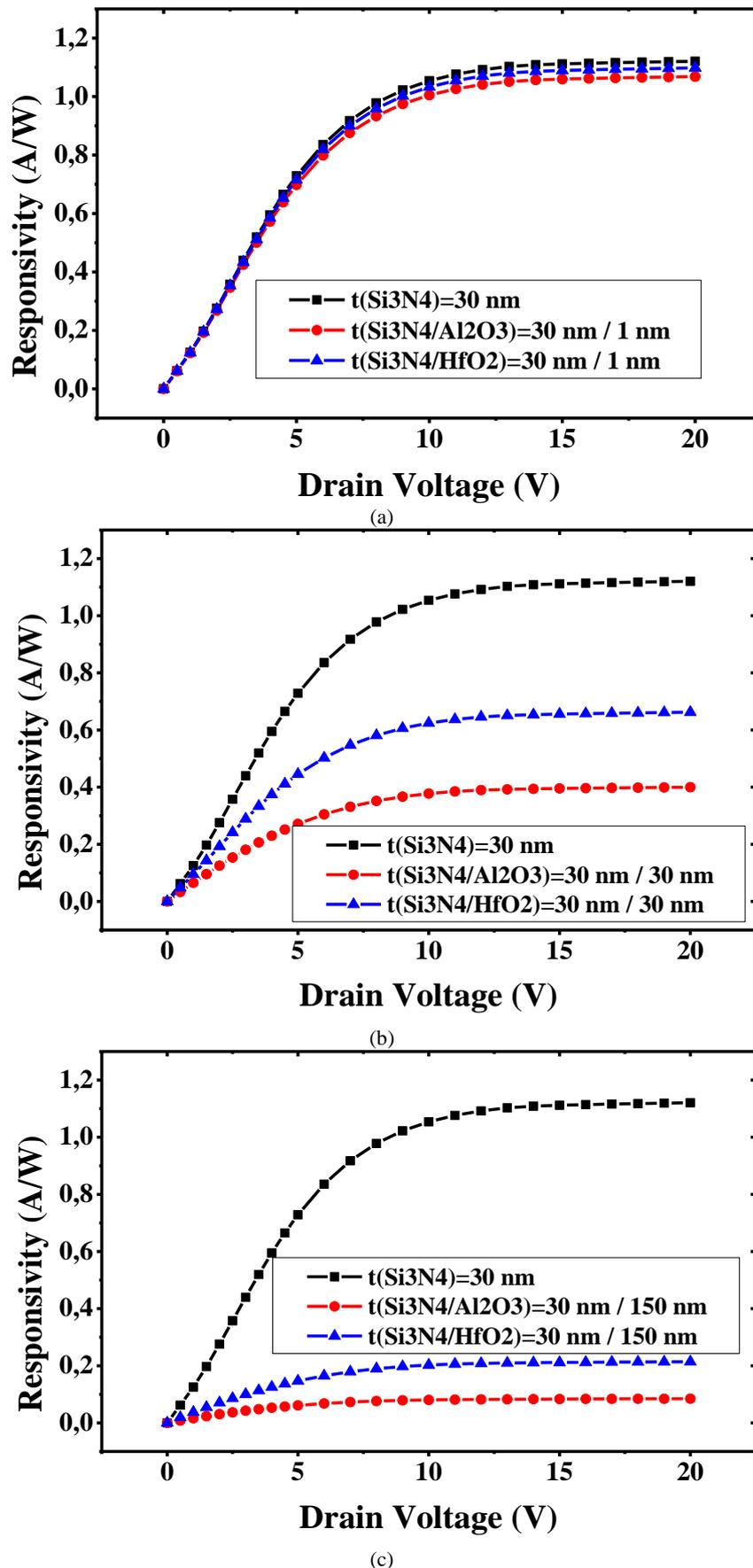


Fig. 16. Responsivity vs drain voltage for the APTs under study illuminated by 420 nm for second dielectric layer thickness of (a) 1nm; (b) 30 nm and (c) 150 nm.

Several facts contributed to the obtained higher than unity EQEs. In addition to the choice of a-Si thickness, many parameters involved in the photogeneration process were investigated. Fig. 17 illustrates the wavelength dependency of EQE (Fig. 17a) and responsivity (Fig. 17b) for different a-Si thicknesses for white light illumination. It clearly appears that the phototransistors selectivity is mainly determined by the material thickness, and that, at 420 nm wavelength, our APTs are very sensitive. They present a maximum response for 300 nm a-Si thickness. In other words, they absorb efficiently the emitted photons so that the dose to which the patient is exposed becomes low.

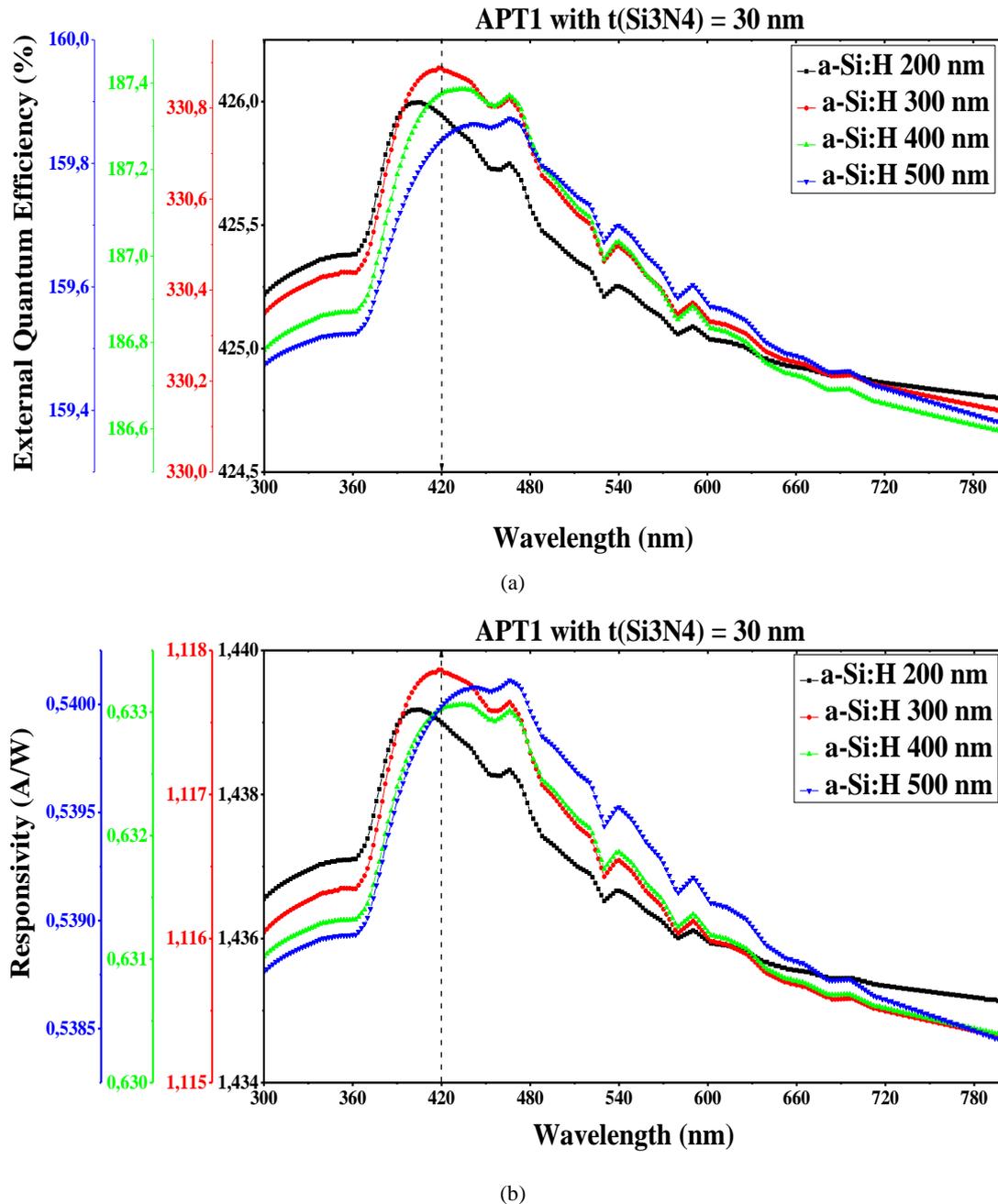


Fig. 17. Wavelength dependency of (a) EQE, and (b) Responsivity for different a-Si thicknesses.

According to equation (7), the EQE is proportional to the photocurrent so that $EQE = k \cdot I_{ph}(V_d)$, where $k = (h \cdot c) / (\lambda \cdot q \cdot P_{inc})$ is a constant and $I_{ph}(V_d)$ is the drain-to-source photocurrent. So, the EQE follows the same trends of the photocurrent. As it is higher than unity, a multiplication process may have occurred in our phototransistors. Even carriers with energies lower than the amorphous silicon bandgap may have contributed to the generation of electron-hole pairs. This phenomenon was experimentally observed and described in [30] and [31], and was attributed to impact ionization by charge carriers. In fact, an extra optical gain may have happened through the flight of the charge carriers to the drain where they are collected. In amorphous silicon transistors, it was found that for higher gate voltages, surface states have negligible effect on I-V characteristics and on the field effect-to-band mobility ratio which gets maximum values [32]. So, during their flight from the source to the drain, the carriers are not subject to trapping effect. Their mean free path becomes longer which results in higher mobility-lifetime product, especially for the chosen a-Si thickness which guarantees a maximum of the number of absorbed photons, as mentioned above and shown in Fig. 17. Thus, carriers acquire enough energies because of collisions in the presence of a high electric field, which leads to an increasing in the number of carriers with high energies capable of causing impact ionization [30] [31]. Effectively Fig. 18, shows the variation of the electric field along the source-to-drain path. It presents a maximum of a 2.41×10^5 V/cm at the drain side region. Very similar values were obtained in [33] and have been demonstrated to be source of impact ionization.

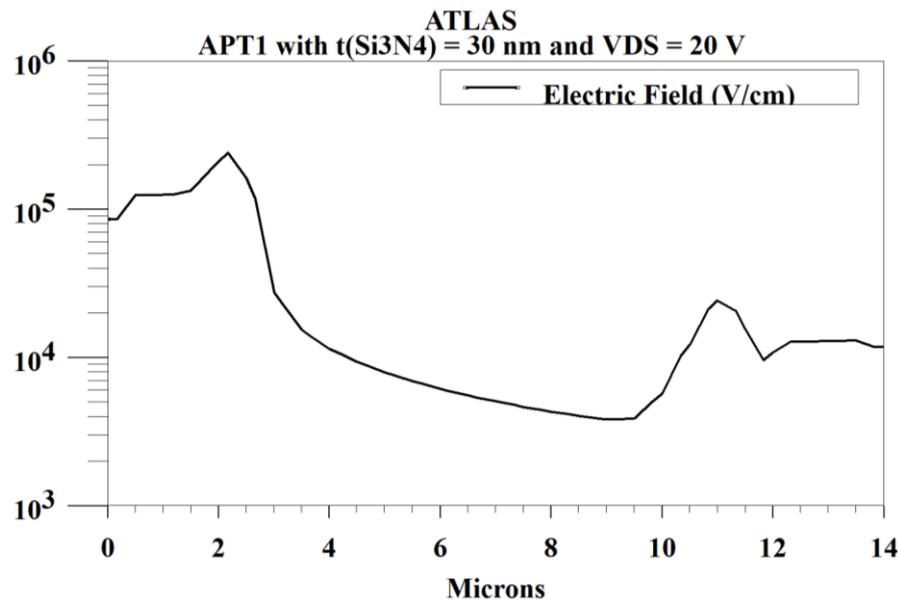


Fig. 18. Electric field variation along the source/drain.

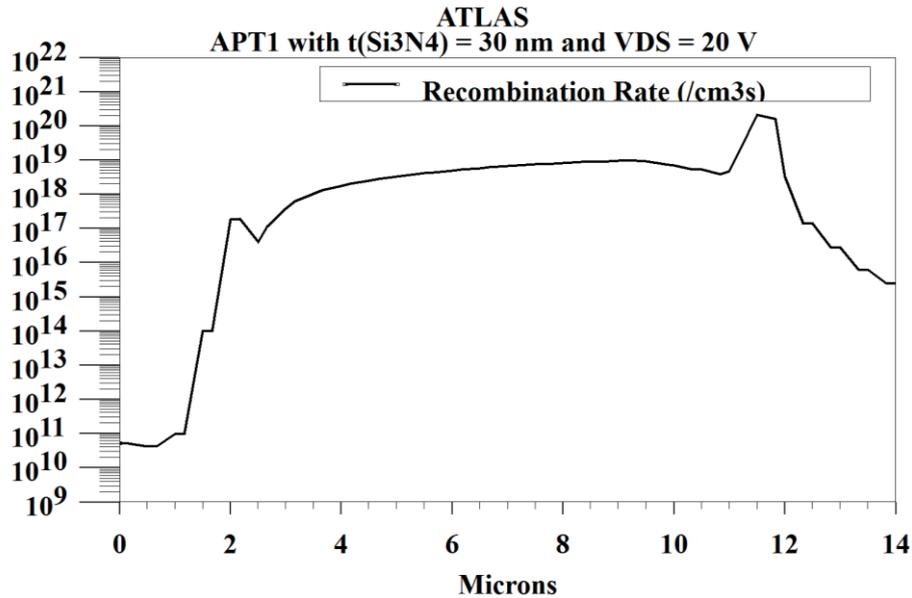


Fig. 19. Recombination rate variation along the source/drain.

The variation of the recombination rate between source and drain regions is illustrated in Fig. 19. A recombination rate peak of 2.21×10^{20} /cm3s is noticed under the source at the contact n+ doped a-Si/intrinsic a-Si. This recombination with the electrons is due to the holes blocked by the built-in potential barrier at this contact. The latter is then reduced by these accumulated holes under the source to lead to a large secondary electron photocurrent by electron injection so that this recombination becomes weaker in the drain region to reduce to 2×10^{17} /cm3s approximately [34]. Even responsivity magnitudes are lower for higher insulators' thicknesses; they remain in the order of reasonable magnitudes for a-Si. They remain very high for thin structures achieving 1.1178 A/W. Comparable results were found in the literature [7], [22], [26]. In [26], responsivity as high as 0.92 A/W was reported for a drain voltage of 10V. In [22], for a-Si:H MSM Photoconductors that are compatible with TFT fabrication, values of 0.18 A/W were obtained for blue light and for an electrode spacing of 5 μ m.

IV. CONCLUSION

Amorphous silicon photo thin-film transistors with double layered insulators using $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ or HfO_2 are reported. Investigations included direct and transfer characteristics in dark and under illumination, generated photocurrents, external quantum efficiency EQE and responsivity R. Performance is evaluated in terms of the dielectric thickness and nature. The $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ transistor shows the lowest off- current comparing with $\text{Si}_3\text{N}_4/\text{HfO}_2$ transistor. The HfO_2 device presents the highest on-current when illuminated. The generated photocurrent is higher for $\text{Si}_3\text{N}_4/\text{HfO}_2$ transistor revealing a lower amount of trapped charge. For very thin thicknesses, under illumination, both devices enhance the Si_3N_4 device off-current and reach Si_3N_4 single layer dielectric based phototransistor performance. EQE and responsivity are higher in HfO_2 devices comparing with Al_2O_3

devices. The results are promising and support further investigations in order to develop high k gate insulators for MIS photo thin-film transistors.

REFERENCES

- [1] K. Rosan, "Hydrogenated Amorphous-Silicon Image Sensors," *IEEE Transactions on Electron Devices*, vol. 36, no. 12, pp. 2923-2927, 1989.
- [2] M. Yamaguchi, Y. Kaneko, and K. Tsutsui, "Two-Dimensional Contact-Type Image Sensor Using Amorphous Silicon Photo-Transistor," *Japanese Journal of Applied Physics*, vol. 32, no. 1B, pp. 458, 1993.
- [3] Z. Hafdi, "An Analytical Capacitance Model for a Hydrogenated Amorphous Silicon Based Thin-Film Transistor," *Physics Procedia*, vol. 21, pp. 122-127, 2011.
- [4] L. Wang, H. Ou, J. Chen, and K. Wang, "A Numerical Study of an Amorphous Silicon Dual-Gate Photo Thin-Film Transistor for Low-Dose X-Ray Imaging," *Journal of Display Technology*, vol. 11, no. 8, pp. 646-651, 2015.
- [5] Rahn, F. Lemmi, J. Lu, P. Mei, R. Apte, R. Street, R. Lujan, R. Weisfield, and J. Heanue, "High Resolution X-Ray Imaging Using Amorphous Silicon Flat-Panel Arrays," in *Nuclear Science Symposium, 1998. Conference Record. 1998 IEEE*, vol. 2. IEEE, pp. 1073-1077, 1998.
- [6] S. M. GadelRab and S. G. Chamberlain, "The Source-Gated Amorphous Silicon Photo-Transistor," *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1789-1794, 1997.
- [7] Y. Vygranenko, A. Nathan, M. Vieira, and A. Sazonov, "Phototransistor with Nanocrystalline Si/Amorphous Si Bilayer Channel," *Applied Physics Letters*, vol. 96, no. 17, pp. 173507, 2010.
- [8] K. Wang, H. Ou, and J. Chen, "Dual-Gate Photosensitive Thin-Film Transistor-Based Active Pixel Sensor for Indirect-Conversion X-Ray Imaging," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2894-2899, 2015.
- [9] M. Yamaguchi, Y. Kaneko, and K. Tsutsui, "Two-Dimensional Contact-Type Image Sensor Using Amorphous Silicon Photo-Transistor," *Japanese Journal of Applied Physics*, vol. 32, no. 1B, pp. 458, 1993.
- [10] S. Martin, C.-S. Chiang, J.-Y. Nahm, T. Li, J. Kanicki, and Y. Ugai, "Influence of the Amorphous Silicon Thickness on Top Gate Thin-Film Transistor Electrical Performances," *Japanese Journal of Applied Physics*, vol. 40, no. 2A, pp. 530, 2001.
- [11] S. Ghanbarzadeh, S. Abbaszadeh, and K. S. Karim, "Low Dark Current Amorphous Silicon Metal-Semiconductor-Metal Photodetector for Digital Imaging Applications," *IEEE Electron Device Letters*, vol. 35, no. 2, pp. 235-237, 2014.
- [12] Y. Kaneko, N. Koike, K. Tsutsui, and T. Tsukada, "Amorphous Silicon Phototransistors," *Applied Physics Letters*, vol. 56, no. 7, pp. 650-652, 1990.
- [13] Z. Hafdi and M. S. Aida, "Modeling and Simulation of Hydrogenated Amorphous Silicon Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 44, no. 3, pp. 1192-1198, 2005.
- [14] Z. Hafdi, "Design Considerations of an Amorphous Silicon Demultiplexer," *Elektronika ir Elektrotechnika*, Vol. 19, No. 8, pp. 65-68, 2013.
- [15] H. Yamamoto, H. Matsumaru, K. Shirahashi, M. Nakatani, A. Sasano, N. Konishi, K. Tsutsui, and T. Tsukada, "A New a-Si TFT With Al₂O₃/SiN Double-Layered Gate Insulator for 10.4-Inch Diagonal Multicolor Display," in *Electron Devices Meeting, 1990. IEDM'90. Technical Digest., International. IEEE*, pp. 851-854, 1990.
- [16] C.-S. Ho, S.-J. Chang, S.-C. Chen, J. J. Liou, and H. Li, "A Reliable Si₃N₄/Al₂O₃-HfO₂ Stack MIM Capacitor for High-Voltage Analog Applications," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2944-2949, 2014.
- [17] Y. Wu, M. Xu, Y. Xuan, P. Ye, J. Li, Z. Cheng, and A. Lochtefeld, "Inversion-Type Enhancement-Mode InP Mosfets with ALD High-K Al₂O₃ and HfO₂ as Gate Dielectrics," in *University/Government/Industry Micro/Nano Symposium, 2008. UGIM 2008. 17th Biennial. IEEE*, pp. 49-52, 2008..
- [18] J. Robertson, "High Dielectric Constant Gate Oxides for Metal Oxide Si Transistors," *Reports on Progress in Physics*, vol. 69, no. 2, p. 327, 2005.
- [19] G. Roll, J. Mo, E. Lind, S. Johansson, and L.-E. Wernersson, "Defect Evaluation in InGaAs Field Effect Transistors with HfO₂ or Al₂O₃ Dielectric," *Applied Physics Letters*, vol. 106, no. 20, p. 203503, 2015.
- [20] Y. Kuo, *Thin film transistors. 1. Amorphous silicon thin film transistors*. Springer Science & Business Media, 2004, vol. 1.
- [21] K. Hiranaka, T. Yoshimura, and T. Yamaguchi, "Effects of The Deposition Sequence on Amorphous Silicon Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 28, no. part 1, pp. 2197-2200, 1989.

- [22] F. Taghibakhsh, I. Khodami, and K. S. Karim, "Characterization of Short-Wavelength-Selective a-Si:H MSM Photoconductors for Large-Area Digital-Imaging Applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 337-342, 2008.
- [23] I. Silvaco, "Atlas User's Manual Device Simulation Software," 2010.
- [24] Y.-T. Tsai, K.-D. Hong, and Y.-L. Yuan, "An Efficient Analytical Model for Calculating Trapped Charge in Amorphous Silicon," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 13, no. 6, pp. 725-728, 1994.
- [25] G. S. Risti_c, "The Digital Flat-Panel X-Ray Detectors," in *Conference on Medical Physics And Biomedical Engineering*, p. 65, 2013.
- [26] M. R. Esmaili-Rad, N. P. Papadopoulos, M. Bauza, A. Nathan, and W. S. Wong, "Blue-Light-Sensitive Phototransistor for Indirect X-Ray Image Sensors," *IEEE Electron Device Letters*, vol. 33, no. 4, pp. 567-569, 2012.
- [27] M. Grodzicka, M. Moszynski, T. Szczesniak, M. Szawlowski, D. Wolski, and J. Baszak, "MPPC Array in the Readout of CsI:Ti, LSO:Ce:Ca, LaBr₃:Ce, and BGO Scintillators," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 3294-3303, 2012.
- [28] E. Takeda, T. Kawaguchi, Y. Nanno, N. Tsutsu, T. Tamura, S.-i. Ishihara, and S. Nagata, "An Amorphous Si TFT Array with TaO_x/SiN_x Double Layered Insulator for Liquid Crystal Displays," in *Display Research Conference, 1988, Conference Record of the 1988 International*. IEEE, pp. 155-158, 1988.
- [29] Y. Lee, I. Omkaram, J. Park, H.-S. Kim, K.-U. Kyung, W. Park, and S. Kim, "A a-Si:H Thin-Film Phototransistor for a Near-Infrared Touch Sensor," *IEEE Electron Device Letters*, vol. 36, no. 1, pp. 41-43, 2015.
- [30] S. D. Ganichev, A. P. Dmitriev, S. A. Emel'yanov, Ya. V. Terent'ev, I. D. Yaroshetskii, and I. N. Yassievich, "Impact ionization in semiconductors under the influence of the electric field of an optical wave," *Soviet Physics—JETP*, vol. 63, no. 2, pp. 445-457, 1986.
- [31] C. -H. Lin, C. W. Liu, "Metal-insulator-semiconductor photodetectors," *Sensors*, vol. 10, no 10, pp. 8797-8826, 2010.
- [32] Z. Hafdi, "Surface States in Amorphous Silicon Thin-Film Transistors: Modeling and Impact," *World Applied Sciences Journal*, vol. 31, pp. 63-68, 2014.
- [33] L. Kuan-Ting, C. Feng-Tso, "High performance raised source/drain thin film transistor with field plate design," *In : Active-Matrix Flat panel Displays and Devices (AM-FPD), 2014 21st International Workshop on*. IEEE, pp. 335-338, 2014.
- [34] Y. Kaneko, N. Koike, K. Tsutsui, T. Sukada, "Amorphous silicon phototransistors," *Applied Physics Letters*, vol. 56, no.7, pp. 650-652, 1990.