A NEW ZCZVT COMMUTATION CELL FOR PWM DC-AC CONVERTERS

C. M. de O. Stein*
cmstein@ieee.org

H. L. Hey†
hey@ctlab.ufsm.br

J. R. Pinheiro†

H. Pinheiro†

H. A. Gründling†

*Federal Center for Technological Education of Paraná - CEFET-PR, 85503-390 - Pato Branco - PR - Brazil.

†Power Electronics and Control Research Group – GEPOC, Federal University of Santa Maria – UFSM, 97105-900 – Santa Maria – RS – Brazil. http://www.ufsm.br/gepoc

ABSTRACT

This paper proposes a new auxiliary commutation cell for PWM inverters that allows the main switches to be turned on and off at zero voltage and zero current. The main switches zero current turn-on reduces the undesired effects of parasitic inductances related to the circuit layout. The main diodes reverse recovery losses are minimized since di/dt and dv/dt are controlled. The ZCZVT commutation cell is located out of the main power path of the converters and is activated only during switching transitions. Additionally, the auxiliary switches are turned on and off at ZCS and use the same ground signals of the upper main switches. The commutation losses are practically reduced to zero. Soft switching operation is guaranteed for full load range without changes in command strategy. The operation of the ZCZVT PWM full-bridge DC-AC Converter is analyzed and an auxiliary commutation cell design procedure based on the analysis is proposed. Experimental results are presented to demonstrate the feasibility of the proposed commutation cell.

Artigo submetido em 02/05/02
1a. Revisão em 15/08/02; 2a. Revisão em 10/03/03
Aceito sob recomendação do Ed. Assoc. Prof. Denizar C. Martins

KEYWORDS: Inverter, soft switching, ZCZVT.

RESUMO

Este artigo propõe um novo circuito auxiliar para inversores PWM que permite que a entrada em condução e o bloqueio das chaves principais ocorram com corrente e tensão nulas. A entrada em condução das chaves principais com corrente nula reduz os efeitos indesejados referentes às indutâncias intrínsecas do circuito. Uma vez que o circuito auxiliar controla o di/dt e o dv/dt, as perdas de recuperação reversa dos diodos principais são minimizadas. A célula de comutação ZCZVT, ativada somente durante as comutações, é localizada fora do caminho principal do fluxo de potência. Adicionalmente, as chaves auxiliares comutam em ZCS e usam o mesmo sinal de terra das chaves principais superiores. Devido à ação do circuito auxiliar, as perdas de comutação são praticamente eliminadas. A operação com comutações suaves é garantida para toda a faixa de carga sem mudanças na estratégia de comando. A operação de um inversor ponte-completa ZCZVT PWM é analizada e, baseado nesta análise, é proposto um procedimento de projeto do circuito auxiliar. Para demonstrar a viabilidade do circuito de comutação proposto, são apresenta-

dos resultados experimentais obtidos em um protótipo.

PALAVRAS-CHAVE: Inversor, comutação suave, ZCZVT.

1 INTRODUCTION

With the growing technology development of power devices, switching mode power conversion moves towards high frequency operation, which can lead to high power density and fast dynamic response. For inverters, in addition to these benefits, operation at high frequency is required to reduce the audible noise, the volume and weight of filters, as well as improved quality of output voltage. However, at high frequency operation, switching losses and electromagnetic interference (EMI) become significant and must be analyzed in detail.

Power semiconductor device commutation can be grouped into two techniques: hard and soft. With hard switching, the devices are required to change their states (on and off), while they are subjected at both finite current and voltage values. High switching stresses produced by the overlapping of voltage and current result in high switching losses. To illustrate the hard switching, figure 1(a) shows the switch voltage and current waveforms. Soft switching techniques aim is to reduce the mentioned overlap between voltage and current during the commutation. Thus it is possible to reduce switching losses, enabling high frequency operation and achieving higher power density, with reduced audible noise, volume and weight of filters, as well as high output voltage quality.

Soft switching techniques can be classified into two groups: zero voltage switching (ZVS) and zero current switching (ZCS) (Hua and Lee, 1995). In the literature, there are a few reviews of soft switching inverters (Bellar et alli, 1998; Pickert and Johnson, 1999; Johnson and Pickert, 1999). The most desirable soft switching scheme is that composed by an auxiliary shunt resonant network, which is activated during the main switches commutation interval only. Therefore, the converter operation is very resembled to that without the auxiliary circuit.

In the literature, several soft switching techniques have been proposed for PWM inverters, and nearly all of them operate with ZVS. Typical examples are the auxiliary resonant commutated pole (ARCP) (Bingen, 1985; McMurray, 1989; De Donker and Lyons, 1990), the ZVS (Barbi and Martins, 1991; Katsis et alii, 1997; Yuan and Barbi, 2000; Lai, 1997b; Pinheiro and Hey, 1996) and ZVT (Zero Voltage Transition) (Choi et alii, 2001) inverters. In these circuits, the auxiliary commutation circuit only helps main switches turn-on, while turn-off losses are reduced by snubber capacitors. Figure 1(b) shows the current and voltage waveforms of a power switch under ZVS. In some ZVS inverters, the load current charges the snubber capacitors at main switches turn-off, and as results, there is an important dependence between the load current value and the conduction time of the main diodes. Moreover, at high power application where minority carrier devices are usually employed, the turn-off losses caused by tail current cannot be totally avoided with ZVS technique (Kutkut et alii, 1995). Minority carrier devices, such as IGBT and MCT, present better performance with zero current switching, which can minimize substantially the turn-off losses mentioned above. Thus, several ZCS techniques applied to PWM inverters, such as ZCT (Zero Current Transition) inverters, have been reported in the literature (Tomasin, 1998; Li et alii, 2000; Li and Lee, 2001). However, main switches turn-on losses and the adverse effects of the main diodes reverse recovery have not yet been not totally solved (Li and Lee, 2001). Moreover, in the ZCT techniques mentioned, the main switches must turn-on at the exact instant that the auxiliary circuit current reaches the output current value. This implies that the main switches command is dependent of the instantaneous value of the output current, resulting in a more complex command circuit. Figure 1(c) shows the ZCS commutation waveforms.

This paper proposes a new auxiliary commutation cell for PWM inverters, denominated Zero Current and Zero Voltage Transition (ZCZVT). This commutation cell allows zero current and zero voltage simultaneously, at both turn-on and turn-off of the main switches. The main switches zero current and zero voltage turn-on can reduce significantly the undesired effects of parasitic inductances and capacitances related to the circuit layout, while the zero current turn-off can minimize substantially the turn-off losses caused by tail current. In addition, since the rates di/dt and dv/dt are reduced, main diodes reverse recovery losses are minimized. Thus, the commutation losses are practically decreased to zero. Additionally, the commutation time is practically independent of the instantaneous output current value, which simplifies the generation of the command signals for the main and auxiliaries switches. To illustrate this class of commutation, the voltage and current waveforms of a power switch are shown in figure 1(d).

The operation of the proposed ZCZVT commutation cell applied to a full-bridge bipolar PWM inverter is theoretically analyzed in Section 2. Section 3 presents design guidelines and a design example. The command circuit

strategy is presented in Section 4. Experimental results obtained from a 1 kW ZCZVT full-bridge IGBT-based inverter are given in Section 5. The last section summarizes the conclusions drawn from this investigation.

2 THE ZCZVT COMMUTATION CELL

Figure 2(a) shows the ZCZVT commutation cell applied to a PWM full-bridge DC-AC converter, which operates with bipolar modulation. The proposed commutation cell is a shunt resonant network made-up of two resonant capacitors C_{R1} and C_{R2}, two resonant inductors L_{R1} and L_{R2}, and two bi-directional auxiliary switch S_{A1}-D_{A1} and S_{A2}-D_{A2}. The auxiliary commutation cell is activated during the switching transitions only.

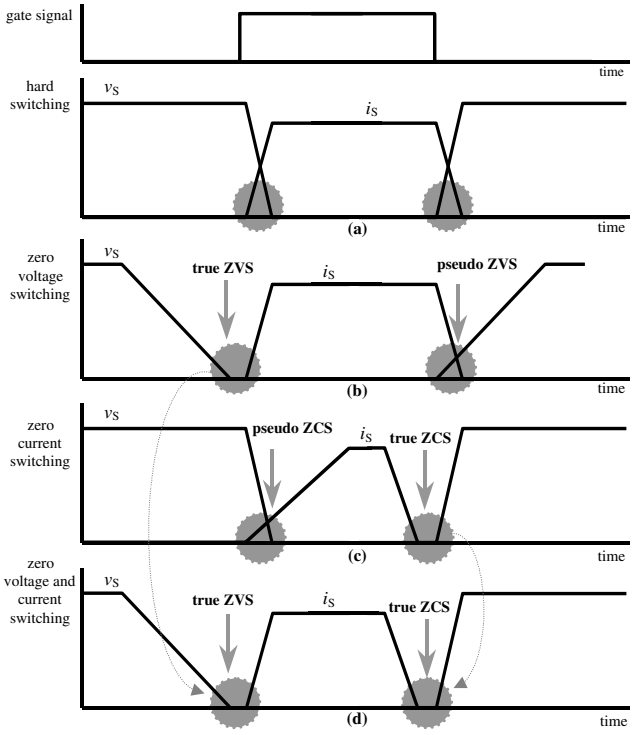


Figure 1: Commutations waveforms.

The proposed commutation technique can be used in three phase circuits, where one commutation cell for each output phase is used. As shown in figure 2(a), the proposed auxiliary circuit is located in parallel with the output filter and the load. Thus, as the ARCP inverter (Lai et alli, 1996; Lai, 1997a), the three phase version of the proposed circuit can be Y or Δ-configured. As the operation of the single phase inverter it can more easily be understood, once less components are involved, in this paper only the ZCZVT PWM full-bridge DC-AC converter operating with bipolar modulation is analysed.

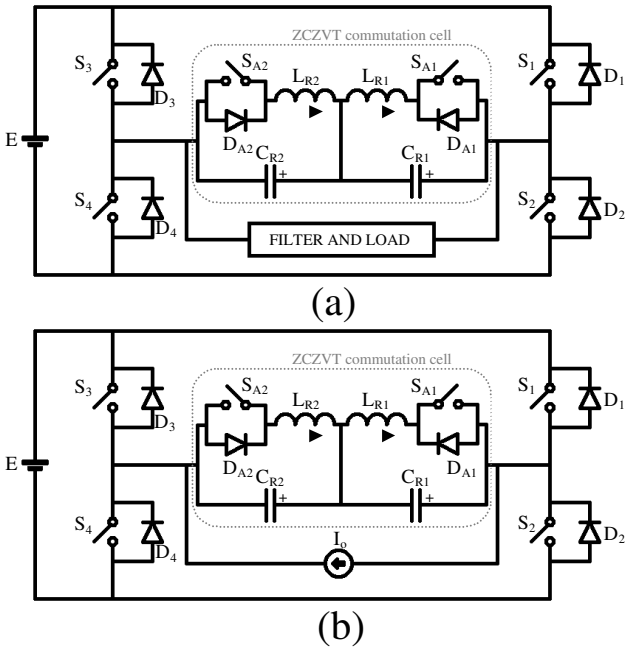


Figure 2: ZCZVT full-bridge converter.

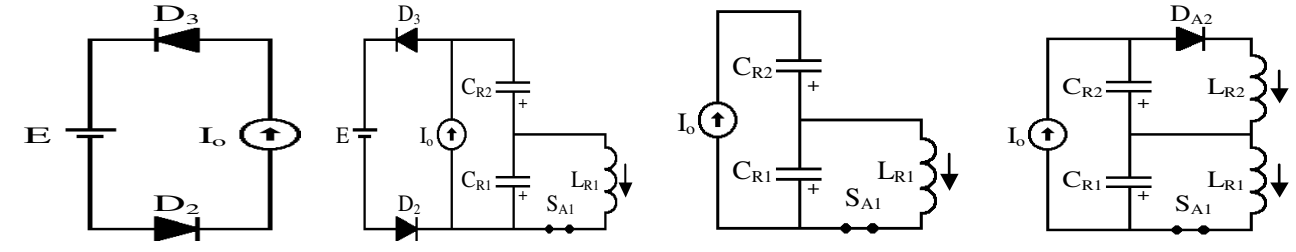
2.1 Principle of Operation

To simplify the analysis, the output current I_o is considered constant into one switching cycle. The operation of the auxiliary commutation circuit is symmetrical for the cases of $I_o < 0$ and $I_o > 0$. So the operation principle will be explained for one case only, i.e., commutations from D_2-D_3 to S_1-S_4 and from S_1-S_4 to D_2-D_3. As shown in figure 3, there are sixteen operating stages during one switching cycle. These stages are described below:

Stage 1. (t_0, t_1) Output current I_o flows through main diodes D_2 and D_3. During this stage the resonant capacitors voltages $v_{CR1}(t)$ and $v_{CR2}(t)$ are clamped at –2E and E respectively.

Stage 2. (t_1, t_2) S_{A1} is turned on under ZCS at t_1. The current through the main diode D_2 decreases due to the resonance among L_{R1}, C_{R1} and C_{R2}. This stage ends when this current reaches zero.

Stage 3. (t_2, t_3) The output current linearly discharges capacitor C_{R2}. The capacitor voltage $v_{CR1}(t)$ increases due to the resonance between L_{R1} and C_{R1}. When$v_{CR2}(t)$ reaches zero, diode D_{A2} begins to conduct.

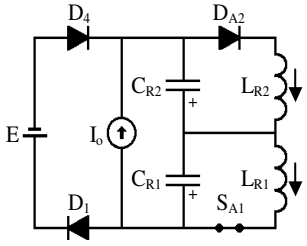


(a) Stage 1 (t_0, t_1)

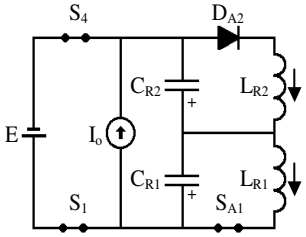
(b) Stage 2 (t_1, t_2)

(c) Stage 3 (t_2, t_3)

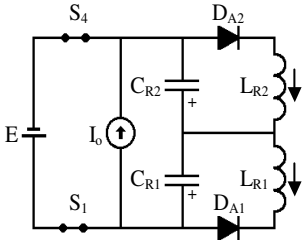
(d) Stage 4 (t_3, t_4)



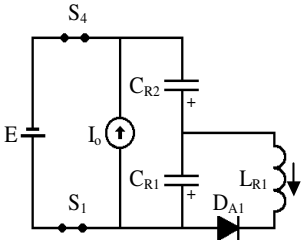
(e) Stage 5 (t_4, t_5)



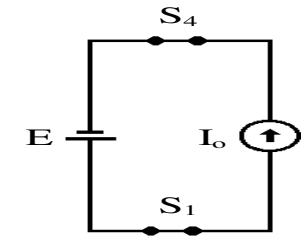
(f) Stage 6 (t_5, t_6)



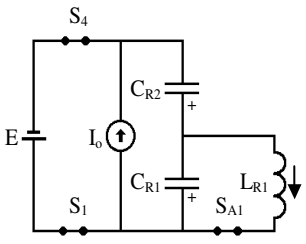
(g) Stage 7 (t_6, t_7)



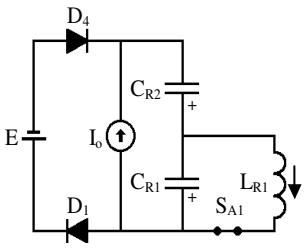
(h) Stage 8 (t_7, t_8)



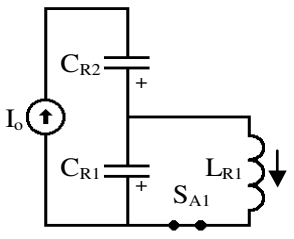
(i) Stage 9 (t_8, t_9)



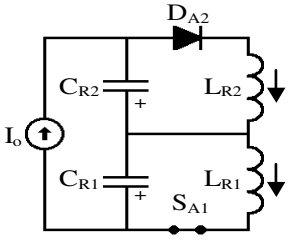
(j) Stage 10 (t_9, t_{10})



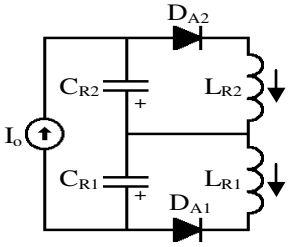
(k) Stage 11 (t_{10}, t_{11})



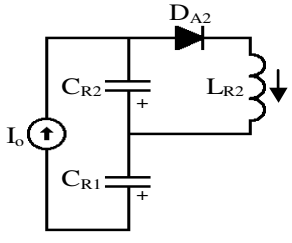
(l) Stage 12 (t_{11}, t_{12})



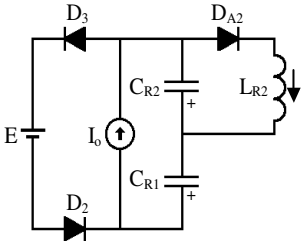
(m) Stage 13 (t_{12}, t_{13})



(n) Stage 14 (t_{13}, t_{14})



(o) Stage 15 (t_{14}, t_{15})



(p) Stage 16 (t_{15}, t_{16})

Figure 3: Operating stages.

Stage 4. (t_3, t_4) The resonant capacitor voltages $v_{CR2}(t)$ $v_{CR1}(t)$ evolve resonantly. When the sum of $v_{CR1}(t)$ and $v_{CR2}(t)$ reaches input voltage, diodes D_1 and D_4 begin to conduct.

Stage 5. (t_4, t_5) To assure ZCS and ZVS, main switches S_1 and S_4 must be turned-on while D_1 and D_4 are conducting. When the current through D_1 and D_4 reaches zero, the main switches S_1 and S_4 begin to conduct.

Stage 6. (t_5, t_6) The current $i_{LR1}(t)$ decreases and when it reaches zero, the diode D_{A1} begins to conduct.

Stage 7. (t_6, t_7) When current $i_{LR2}(t)$ reaches zero, diode D_{A2} turns off. To assure ZCS and ZVS, the auxiliary switch S_{A1} must be turned off during this stage.

Stage 8. (t_7, t_8) When current $i_{LR1}(t)$ reaches zero, diode D_{A1} turns off.

Stage 9. (t_8, t_9) Operation circuit at this stage is similar to that of hard-switching PWM full-bridge converter. Output current I_o flows through main switches S_1 and S_4.

Stage 10. (t_9, t_{10}) The auxiliary switch S_{A1} is turned on again under ZCS at t_9. The current $i_{LR1}(t)$ increases due to the resonance among L_{R1}, C_{R1} and C_{R2}. When the current through the main switches S_1 and S_4 reaches zero, the diodes D_1 and D_4 begin to conduct. The voltage across main switches S_1 and S_4 are clamped at zero.

Stage 11. (t_{10}, t_{11}) The resonance evolves until the current through the main diodes D_1 and D_4 reaches zero. To assure ZVS and ZVS, the gate signals of main switches S_1 and S_4 must be removed during this stage.

Stage 12. (t_{11}, t_{12}) The capacitor C_{R2} is linearly discharged to zero by output current. At this moment diode D_{A2} begins to conduct.

Stage 13. (t_{12}, t_{13}) The resonant inductor current $i_{LR1}(t)$ decrease due to the resonance among L_{R1}, L_{R2}, C_{R1} and C_{R2}. When the current $i_{LR1}(t)$ reaches zero, the diode D_{A1} begins to conduct.

Stage 14. (t_{13}, t_{14}) The resonance continues. When the current $i_{LR1}(t)$ reaches zero again, the diode D_{A1} is turned off naturally.

Stage 15. (t_{14}, t_{15}) The capacitor C_{R1} is linearly discharged by the output current and the resonant capacitor voltage $v_{CR2}(t)$ increase due to the resonance between L_{R2} and C_{R2}. When the sum of the resonant capacitor voltages $v_{CR1}(t)$ and $v_{CR2}(t)$ reaches the negative of the input voltage, the diodes D_2 and D_3 begin to conduct.

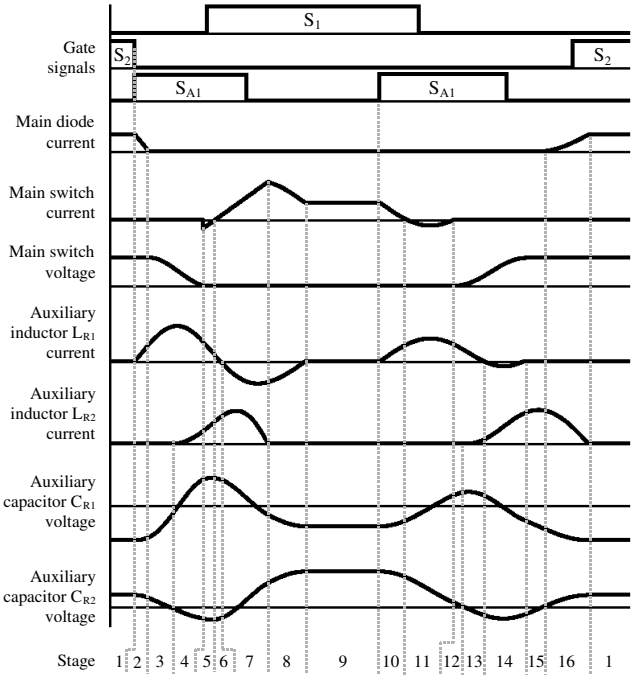


Figure 4: Theoretical waveforms.

Stage 16. (t_{15}, t_0) The resonant inductor current $i_{LR2}(t)$ decrease due to the resonance among L_{R2}, C_{R1} and C_{R2}. When the resonant inductor current $i_{LR2}(t)$ reaches zero the diode D_{A2} turns off, beginning another switching cycle.

Figure 4 shows the theoretical waveforms of the converter operation.

3 RESONANT TANK DESIGN GUIDELINES AND EXAMPLE

This section presents a design procedure and an example to determine the resonant tank elements values of the proposed ZCZVT commutation cell. The given inverter specifications consists of:

Input Voltage	$E = 200$ V
Output Power	$P_o = 1000$ W
Output Voltage	$V_o = 110$ Vrms
Output Current Ripple	$\Delta I = 20\%$

The design procedure consists of four steps, which are:

a) Find the output current peak from the specifications:

$$I_o = \frac{\sqrt{2}P_o}{V_o}(1 + \Delta I) \quad (1)$$

b) Determine the characteristic impedance. To assure main switches turn-off under ZCS and ZVS, during stages 10 and 11, the current peak diverted from main switch to auxiliary circuit must be larger than the output current peak. From these stages, the current peak through capacitor C_{R2} is given by:

$$I_{pk} = \frac{E}{\sqrt{2}Z}. \quad (2)$$

By equations (1) and (2), a parameter k can be defined as follows:

$$k = \frac{I_{pk}}{I_o}, \quad \text{where} \quad k \geq 1. \quad (3)$$

By using equations (2) and (3), the characteristic impedance Z can be defined as:

$$Z = \frac{E}{\sqrt{2}kI_o}. \quad (4)$$

c) Determine the resonant frequency. To minimize main diodes reverse recovery, resonant frequency of stage 2 can be chosen to control the di/dt during turn-off. The di/dt of main diodes at stage 2 can be approximate by:

$$\frac{di}{dt} \approx \frac{I_o\omega}{\sqrt{2}asin\left(\frac{1}{2k}\right)}. \quad (5)$$

By using equation (5), the resonant frequency ω can be obtained as follows:

$$\omega = \frac{\frac{di}{dt}\sqrt{2}asin\left(\frac{1}{2k}\right)}{I_o}. \quad (6)$$

d) Compute the tank resonant components values. From equations (4) and (6), the resonant components values can be defined as follows:

$$L_{R1} = L_{R2} = \frac{Z}{\omega} = \frac{E}{2k\frac{di}{dt}asin\left(\frac{1}{2k}\right)}, \quad (7)$$

$$C_{R1} = C_{R2} = \frac{1}{Z \cdot \omega} = \frac{kI_o^2}{E\frac{di}{dt}asin\left(\frac{1}{2k}\right)}. \quad (8)$$

By equations (7) and (8), choosing $k = 1.1$, which is a practical design value to compensate parasitic losses, and adopting a di/dt of 80 A/μs (Jovanovic and Jang, 2000), the resonant components values can be calculated:

$$L_{R1} = L_{R2} = \frac{Z}{\omega} = 2.4\mu H, \quad (9)$$

$$C_{R1} = C_{R2} = \frac{1}{Z \cdot \omega} = 34.7nF. \quad (10)$$

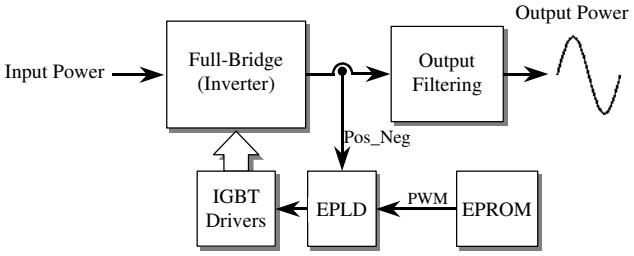


Figure 5: Block diagram of the command and power circuits.

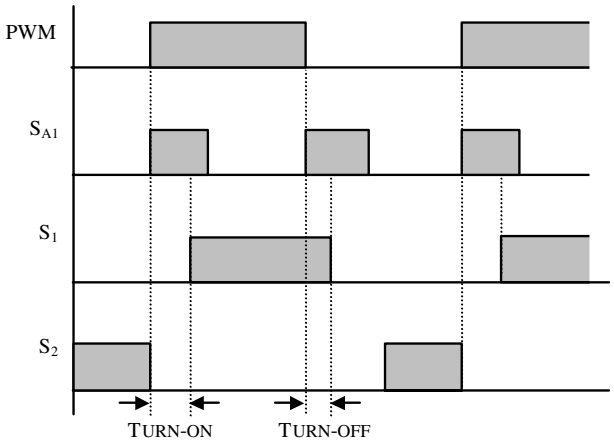


Figure 6: Command circuit waveforms.

4 COMMAND CIRCUIT STRATEGY

Table 1: Utilized Components and Parameters

Component	Parameter
V_{in} (input voltage)	200 V
L_{R1} and L_{R2}	2.5 μH
C_{R1} and C_{R2}	33 nF
L (output filter)	500 μH
C (output filter)	4 μF
R (load)	12 Ω

The block diagram of the open-loop command circuit for the full-bridge ZCZVT inverter presented in this paper is shown in figure 5. It is composed of an EPROM,

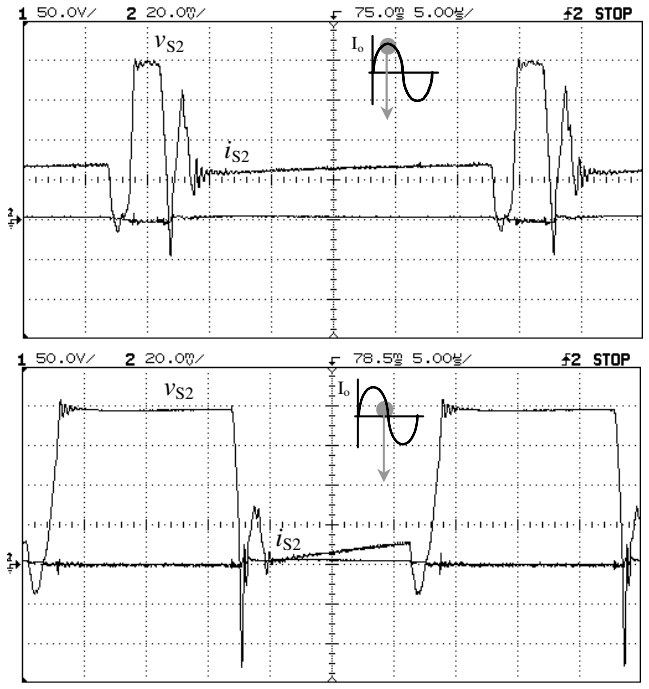


Figure 7: Main switch S2 voltage and current. (scales: 50 V/div.; 10A/div.; 5ms/div.)

where the PWM signal is recorded, and an Erasable Programmable Logic Device (EPLD). The simplicity and programmability of the EPLD make it a good choice for prototyping digital systems. With the PWM and the output current direction, the gate signals are generated in the EPLD. Figure 6 shows the PWM and the gate signals generated in the command circuit represented in figure 5 for $I_o > 0$. For $I_o < 0$, the main switches gate signals are swapped, and auxiliary switch S_{A2} is used instead of S_{A1}. As the commutation time is practically independent of the instantaneous output current value, the auxiliary switches conduction times and the delay times between the gate signals of the main and auxiliary switches are constant.

5 EXPERIMENTAL RESULTS

Following the design example shown in the preceding section, a full-bridge inverter laboratory prototype has been implemented to verify the operation of the proposed ZCZVT commutation cell. The power stage circuit is shown in figure 2(a), and the components and parameters used are summarized in Table I. The active switches were implemented with an UFS (ultrafast switches) series IGBTs from Intersil Semiconductors, which present built-in antiparallel hyperfast diodes. The open-loop command circuit has been implemented using

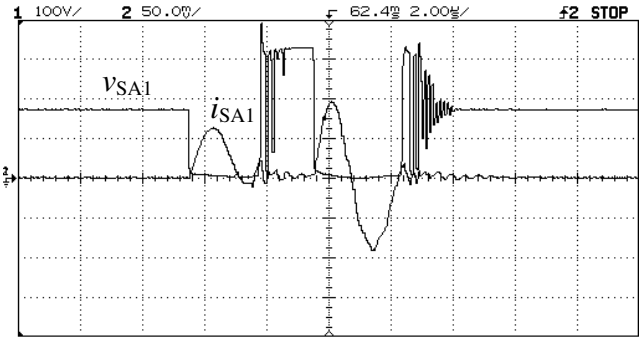


Figure 8: Auxiliary switch SA1 voltage and current. (scales: 100 V/div.; 25A/div.; 1ms/div.)

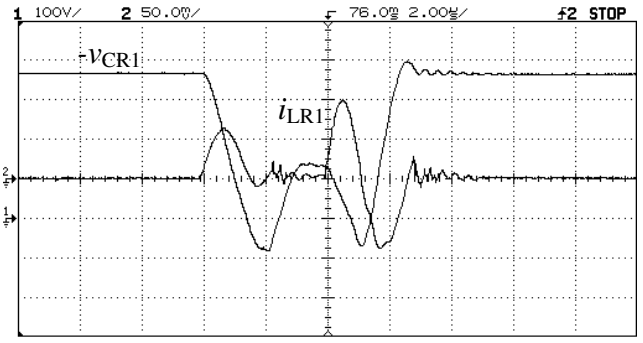


Figure 9: Resonant elements waveforms (iLR1(t) and -vCR1(t)). (scales: 100 V/div.; 25A/div.; 1ms/div.)

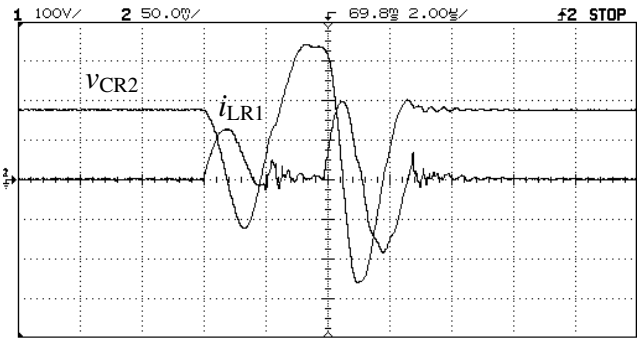


Figure 10: Resonant elements waveforms (iLR1(t) and vCR2(t)). (scales: 100 V/div.; 25A/div.; 1ms/div.)

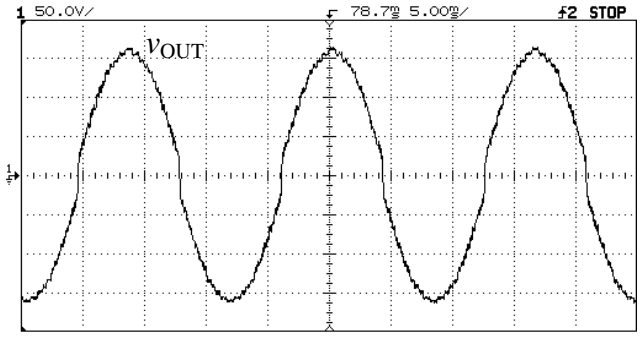


Figure 11: Output voltage. (scales: 50 V/div.; 5ms/div.)

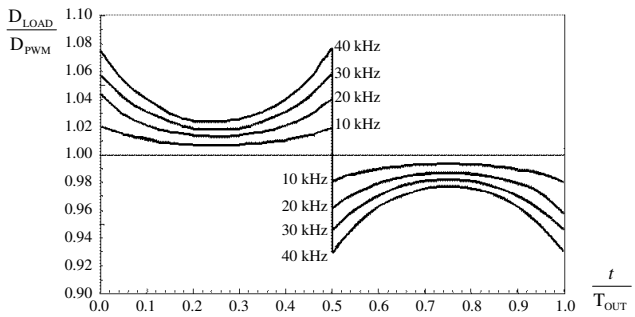


Figure 12: Variation of duty-cycle over an output voltage period.

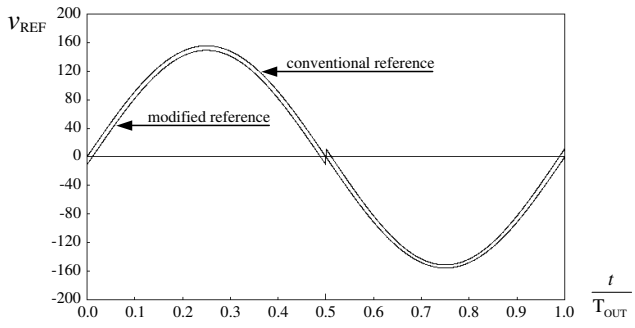


Figure 13: Reference signals.

a single EPLD EPM7128SLC84-15 from Altera Corporation.

Figures 7, 8, 9, 10 and 11 show the experimental waveforms obtained at full load. They confirm the analysis made in Section 2. As can be seen in figure 7, the commutations of the main switchesoccurs truly without losses, i.e., with ZCZVS for full load range. This is a very interesting feature introduced by the ZCZVT commutation cell. Due to the slowed di/dt, main diodes reverse recovery losses are negligible. Figure 8 shows zero current switching of the auxiliary switch S_{A1}. Figures 9 and 10 show the waveforms of the resonant elements.

Figure 11 shows the output voltage of the converter. As can be seen, there is a distortion in the output voltage waveform, where close to zero crossing is observed. This distortion occurs because the converter output voltage stays with the same polarity even after the PWM signal to have changed, and is a consequence of the action of the auxiliary commutation cell. Thus, the load duty cycle (D_{LOAD}) is not equal to the PWM duty cycle (D_{PWM}). This distortion always occurs either when a commutation cell is inserted in the circuit, or when a dead time is added between the command signals of the switches. In the literature, there is no references describing this effect caused by the use of commutation cells. Dodson et alli (1990) revise the origin of the distortion caused by the dead time, as well as present forms to attenuate it. Figure 12 shows the variation of duty cycle of ZCZVT converter over the output voltage period. As can be seen, the relationship between the load duty cycle and the PWM duty cycle is directly proportional to the switching frequency of the converter.

To compensate the variation in the modulation due to the action of the auxiliary commutation cell, a modified PWM signal was generated. Figure 13 shows the conventional reference signal together with the modified signal. These reference signals are for amplitude modulation ratio of 0.778 and a switching frequency of 30 kHz. Figure 14 shows the output voltage obtained with the ZCZVT full bridge converter operating with the modified PWM signal. Alternatively, the output voltage distortion can be solved with a closed loop operation.

The efficiency curve of the inverter is shown in figure 15. For hard operation, the efficiency diminishes with the power increase, due to the increase of the conduction and commutation losses of the converter. With the addition of the proposed soft switching commutation cell, the inverter presents higher efficiency. It should be noticed in figure 15 that efficiency grows with the increase of output power until the nominal level. This character-

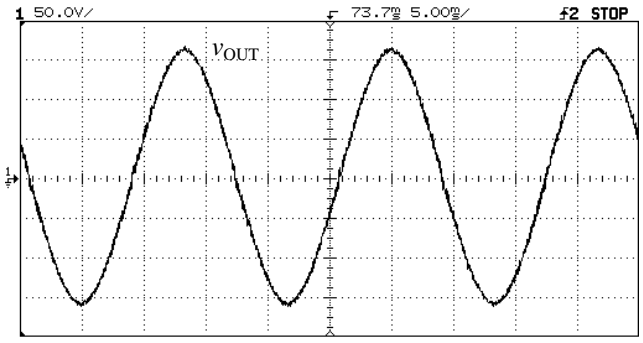


Figure 14: Output voltage.(scales: 50 V/div.; 5ms/div.)

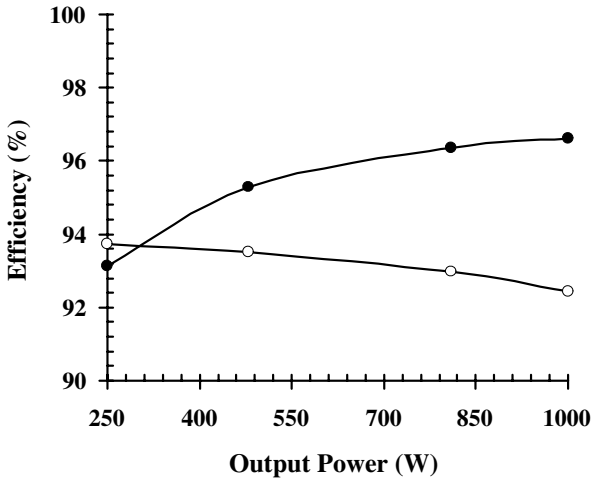


Figure 15: Efficiency curve.○ Hard version; • Soft version

istic is because the energy involved with the commutation cell is practically constant over all the output power range.

6 CONCLUSIONS

This paper proposes a new ZCZVT full-bridge bipolar PWM inverter. Operating principles have been described and verified by experimental results obtained from a 30 kHz laboratory prototype rated at 1 kW, input voltage of 200V and output voltage of 110Vrms. The experimental results demonstrate that the design procedure proposed is adequate, guaranteeing the correct converter operation.

Soft switching for all power semiconductor devices is achieved. The main switches commutate under ZCS and ZVS simultaneously at both turn-on and turn-off. This commutation technique is therefore suitable for both minority and majority carrier semiconductor device applications such as Power MOSFETs, IGBTs, MCTs, Thyristors etc. In addition, the auxiliary switches commutate under ZCS at turn-on and under ZCS and ZVS at turn-off and the main diodes are commutated under ZVS.

The ZCZVT commutation cell is placed out of the main power path of the converters and is activated during the switching transitions only. Additionally, the auxiliary switches use the same ground signal of the upper main switches, and the converter operates with slow di/dt and dv/dt on power devices, reducing the circuitry noises, and parasitic oscillations.

ACKNOWLEDGMENT

The authors would like to express their special thanks to *Icotron – an EPCOS Company* for material support.

REFERENCES

Barbi, I. and D. C. Martins (1991). A true PWM zero-voltage switching pole with very low additional RMS current stress. *IEEE Power Electronics Specialist Conference*, pp. 261-267.

Bellar, M. D., T. S. Wu, A. Tchamdjou, J. Mahdavi and M. Ehsani (1998). A review of soft-switched dc-ac converters. *IEEE Transactions on Industry Applications*, Vol. 34, No. 4, pp. 847-860.

Bingen, G. (1985). Utilisation de transistors a fort courant et tension elevee. *First European Confer-*

ence on Power Electronics and Applications, Vol. 1, pp. 1.15-1.20.

Choi, J. Y., D. Boroyevich, J. Francis and F. C. Lee (2001). A novel ZVT inverter with simplified auxiliary circuit. *IEEE Applied Power Electronics Conference*, pp. 1151-1157.

De Donker, R. W. and J. P. Lyons (1990). The auxiliary resonant commutated pole converter. *IEEE Industry Applications Society Annual Meeting Record*, pp. 1228-1235.

Dodson, R. C., P. D. Evans, H. T. Yazdi and S. C. Harley (1990). Compensation for dead time degradation of PWM inverter waveforms. *IEE Proceedings B – Electric Power Applications*, Vol. 137, No. 2, pp. 73-81.

Hua, G. and F. C. Lee (1995). Soft-switching techniques in PWM converters. *IEEE Transactions on Industrial Electronics*, Vol. 42, No. 6, pp. 595-603.

Johnson, C. M. and V. Pickert (1999). Three-phase soft-switching voltage source converters for motor drives. Part 2: Fundamental limitations and critical assessment. *IEE Proceedings B – Electric Power Applications*, Vol. 146, No. 2, pp. 155-162.

Jovanovic, M. M. and Y. Jang (2000). A novel active snubber for high-power boost converters. *IEEE Transactions on Power Electronics*, Vol. 15, No. 2, pp. 278-284.

Katsis, D. C., M. A. Herwald, J.-Y. Choi, D. Boroyevich and F. C. Lee (1997). Drive cycle evaluation of a soft-switched electric vehicle inverter. *Annual Conference of the IEEE Industrial Electronics Society*, pp. 658-663.

Kutkut, N. H.; D. M. Divan, D. W. Novotny and R. Marison (1995). Design considerations and topology selection for a 120 kW IGBT converter for EV fast charging. *IEEE Power Electronics Specialist Conference*, pp. 238-244.

Lai, J. S., R. W. Young, G. W. Ott, J. W. McKeever and F. Z. Peng (1996). A delta configured auxiliary resonant snubber inverter. *IEEE Transactions on Industry Applications*, Vol. 32, No. 3, pp. 518-525.

Lai, J. S. (1997a). Fundamentals of a new family of auxiliary resonant snubber inverters. *Annual Conference of the IEEE Industrial Electronics Society*, pp. 645-650.

Lai, J. S. (1997b). Resonant snubber-based soft-switching inverters for electric propulsion drives", *IEEE Transactions on Industrial Electronics*, Vol. 44, No. 6, pp.71-80.

Li, Y. and F. C. Lee (2001). A comparative study of a family of zero-current-transition schemes for three-phase inverter applications. *IEEE Applied Power Electronics Conference*, pp. 1158-1164.

Li, Yong, F. C. Lee, J. S. Lai and D. Boroyevich (2000). A novel three-phase zero-current-transition and quasi-zero-voltage-transition (ZCT-QZVT) inverter/rectifier with reduced stresses on devices and components. *IEEE Applied Power Electronics Conference*, pp. 1030-1036.

McMurray, W. (1989). Resonant snubbers with auxiliary switches. *IEEE Industry Applications Society Annual Meeting Record*, pp. 829-834.

Pickert, V. and C. M. Johnson (1999). Three-phase soft-switching voltage source converters for motor drives. Part 1: Overview and analysis. *IEE Proceedings B – Electric Power Applications*, Vol. 146, No. 2, pp. 147-154.

Pinheiro, J. R. and H. L. Hey (1996). An active auxiliary commutation circuit for inverters. *IEEE Power Electronics Specialists Conference*, pp. 223-229.

Tomasin, P. (1998). A novel topology of zero-current-switching voltage-source PWM inverter for high-power applications. *IEEE Transactions on Power Electronics*, Vol. 13, No. 1, pp. 186-193.

Yuan, X. and I. Barbi (2000). Analysis, designing, and experimentation of a transformer-assisted PWM zero-voltage switching pole inverter. *IEEE Transactions on Power Electronics*, Vol. 15, No. 1, pp. 72-82.