AN IMPROVED DESIGN FOR ZVT DC-DC PWM CONVERTERS WITH SNUBBER ASSISTED AUXILIARY SWITCH

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ABSTRACT

This paper proposes an improved design to calculate the snubber auxiliary elements of ZVT DC-DC PWM converters with snubber assisted auxiliary switch. The proposed improved design guidelines are based on the reduction of the conduction losses through the auxiliary circuit. It is accomplished by the unique location of the turn-off snubber capacitor, which is shared by both active switches. By means of this improved design guidelines the converter efficiency can be increased.

An efficiency comparative analysis is carried out and the experimental results, obtained from 1 kW, 100 kHz laboratory prototypes, show a relevant improvement in converter efficiency compared to the original converter design. In addition, experimental results also confirm that with the improved design the ZVT PWM converters with snubber assisted auxiliary switch can be competitive with ZVT PWM converters with constant auxiliary voltage source (True PWM ZVS pole).

KEYWORDS: Soft-switching, ZVT, converters design.

RESUMO

Este artigo propõe uma metodologia de projeto aprimorada para determinação dos componentes auxiliares para o conversor ZVT CC-CC PWM snubber assisted auxiliary switch. O procedimento de projeto proposto é baseado na redução das perdas de condução no circuito auxiliar. Isto é somente possível devido à localização do capacitor snubber de bloqueio, o qual é compartilhado por ambas as chaves ativas. Através do procedimento de projeto proposto o rendimento do conversor pode ser aumentado.

Uma análise comparativa do rendimento é apresentada e os resultados experimentais, obtidos de protótipos de laboratório de 1 kW, 100 kHz, mostram uma melhoria relevante em relação ao rendimento apresentado pelo projeto original. Além disso, os resultados experimentais também confirmam que o projeto proposto para o conversor ZVT snubber assisted auxiliary switch torna-o competitivo em relação ao conversor ZVT PWM com fonte auxiliar de tensão constante (true PWM ZVS pole).

PALAVRAS-CHAVE: Comutação suave, ZVT, projeto de conversores.

1 INTRODUCTION

With the aim of obtaining an improvement in overall performance of the PWM converters and further a reduction in size and weight of these power converters, soft-switching techniques have been the subject of intensive research. These techniques allow the power converters to operate with higher switching frequencies without penalizing the trade-off between switching losses and converter efficiency. Among these techniques, the commutation under Zero Voltage Transition – ZVT has been frequently employed, mainly when the active switches are implemented with majority carrier semiconductor devices. Besides the enhanced switching conditions for main devices, this technique also provides the absorption of main devices intrinsic capacitances. Moreover, the ZVT cell is placed in parallel with the main power path, enabling the converter to

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operate as close as possible to its PWM counterpart, with low conduction losses when compared to other Zero Voltage Switching - ZVS techniques (Hua *et al*., 1995).

In spite of ZVT converter proposed by (Hua *et al*., 1992) presents many advantages, its auxiliary circuit promotes inadequate commutation conditions to auxiliary switch. When auxiliary switch is implemented using power MOSFET devices, its output intrinsic capacitance enables Zero Voltage Switching - ZVS turn-off. Nevertheless, the energy stored during this process is totally dissipated when the switch is turned on reducing the efficiency gain of the soft switching approach (Erickson and Maksimovic, 2001). On the other hand, when IGBT devices are used, the turn-on capacitive losses are minimized but the turn-off losses associated with its current tail are not effectively reduced (Filho *et al.*, 1994), which further limits its frequency operation.

Recently, several topologies have been proposed to minimize this inconvenient characteristic, which are based on one of the following principles:

a) Addition of a DC voltage source in series with the auxiliary switch S_a (Martins *et al.*, 1993; Gegner and Lee, 1994; Gegner and Lee, 1994; Lee, *et al.*, 1998; Filho, *et al.*, 1994), yielding zero-current switching (ZCS) conditions to this switch. As ZCS switching conditions are well suited to IGBT devices the turn-on capacitive losses are quite reduced. Moreover, depending on the value of the DC voltage source, a reduction in reactive energy can be accomplished. Therefore, the conduction losses can be minimized. Nevertheless, the implementation of the auxiliary DC voltage source is done by means of (i) a voltage transformer (Martins *et al.*, 1993; Gegner and Lee, 1994; Gegner and Lee, 1994; Lee, *et al.*, 1998) or (ii) a converter voltage source or sink (Filho, *et al.*, 1994), which can result in (i) demagnetizing problems and EMI degradation or (ii) operation under limited voltage ratio conversion;

b) Addition of a resonant circuit in series with the auxiliary switch also yields in ZCS conditions to this switch. Although low switching losses are achieved, the additional current stresses on main switch and/or additional voltage stresses on auxiliary switch (Yang and Lee, 1993; Moschopoulos *et al.*, 1995; Tseng and Chen, 1998; Xu *et al*., 2000; Jain *et al.*, 2001), resulting from the resonant tank operation, enlarge the converter conduction losses.

c) Addition of passive turn-off snubbers to the auxiliary switch (Streit and Tollik, 1991; Yaakov *et al.*, 1995; Liu *et al.*, 2000; Kim *et al.*, 2000; Menegáz *et al.*, 1999), which can effectively improve the switching conditions to auxiliary switch. However, they cannot avoid the turn-on capacitive losses due to parasitic capacitance present in auxiliary switch (MOSFET).

As it can be seen, none of the above mentioned solutions could enhance the ZVT features without adding some drawback. However, by the efficiency point of view, the reduction of reactive energy makes ZVT converters with auxiliary DC voltage source more attractive (Martins *et al.*, 1993; Gegner and Lee, 1994; Gegner and Lee, 1994; Lee, *et al*., 1998; Filho, *et al.*, 1994).

In spite of this fact, if the storage energy in both, main and auxiliary switch turn-off snubbers, is not discharged by the auxiliary inductor, instead of, being directly regenerated to the output, the conduction losses can be quite reduced. This way, ZVT converters with snubber assisted auxiliary switch can be as attractive as ZVT with auxiliary DC voltage source, without any inconvenient related to the DC voltage source implementation.

To accomplish these features, the ZVT DC-DC PWM converter with snubber assisted auxiliary switch presented in (Streit and Tollik, 1991; Yaakov *et al.*, 1995; Liu *et al.*, 2000), also referred as Flying Capacitor ZVT converter, was designed in such way that the auxiliary inductor and turn-off snubber capacitors for main and auxiliary switches are independent of each other, ensuring that there is no trade-off among the choice of their values. Therefore, they can be truly optimized, improving the converter efficiency performance.

This paper is organized as follows: Section 2 describes the ZVT PWM converters with snubber assisted auxiliary switch, as well as its operation principle. Section 3 presents an improved snubber design to calculate the snubber for the auxiliary switch. In Section 4 a comparative analysis between the original and the proposed design are carried out. Section 5 presents the comparative experimental results obtained from three ZVT PWM boost laboratory prototypes. Finally, Section 6 presents the conclusions from the analysis and the experimental results.

2 ZVT PWM CONVERTERS WITH SNUBBER ASSISTED AUXILIARY SWITCH - SAAS

The common DC-DC PWM switching cell, Fig. 1(a), can be used to derive every DC-DC PWM converter topology. Hence, to obtain a generalized analysis of the commutation process, this circuit, presented in (Zhu and Ding, 1999), is adopted. Assuming that the filter inductance L (L_1) is large enough, the current can be considered constant during one switching period of the PWM converter. Therefore, its circuit can be simplified as depicted in Fig. 1(b).

Fig 2 shows the snubber assisted auxiliary circuit added to the boost converter derived from the common DC-DC PWM switching cell. It can be seen that the auxiliary circuit is composed by: an active current unidirectional switch S_a-

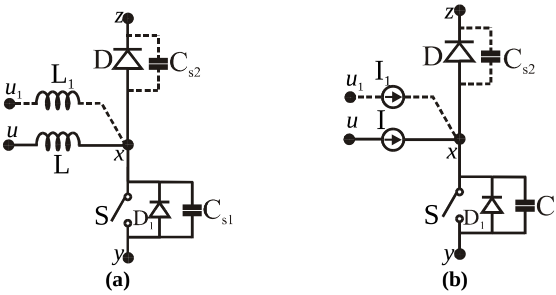


Figure 1. General PWM converter diagram. (a) Basic PWM switching cell; (b) Simplified PWM switching cell.

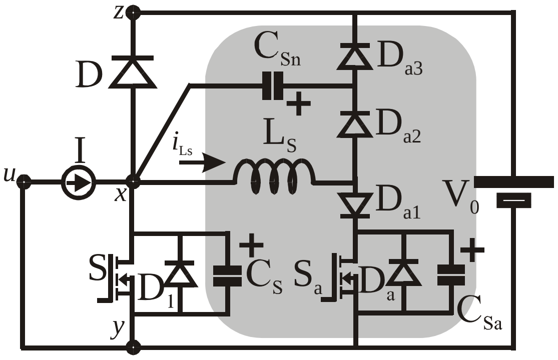


Figure 2. ZVT PWM Boost Converter with SAAS.

D_{a1}; two bypass diodes D_{a2} and D_{a3}; a snubber inductor L_S; a snubber capacitor C_{Sn}; and the intrinsic switches output capacitances C_S and C_{Sa}. In steady-state operation the converter assumes nine circuit modes, Fig 3. The operation of each mode is described as follows.

Mode 0 ($t \leq t_0$)**:** Before t_0, both switches are off and current I flows through diode D. The converter PWM modulation defines the time for this mode. During this operation mode C_{Sn} is discharged and C_S and C_{Sa} are charged to V_{ZY}.

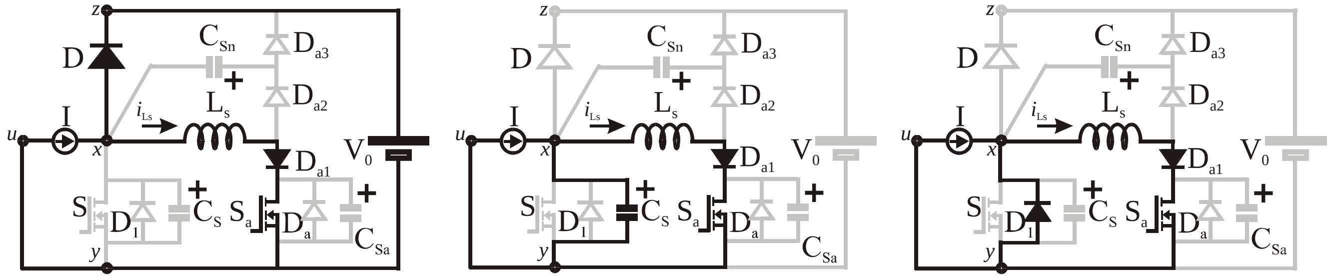
Mode 1 ($t_0 < t \leq t_1$)**:** At t_0 auxiliary switch S_a is turned on with ZCS conditions and auxiliary inductor, currents i_{ls} increases linearly with the following ratio.

$$i_{Ls} = V_{ZY} t / L_S \qquad (1)$$

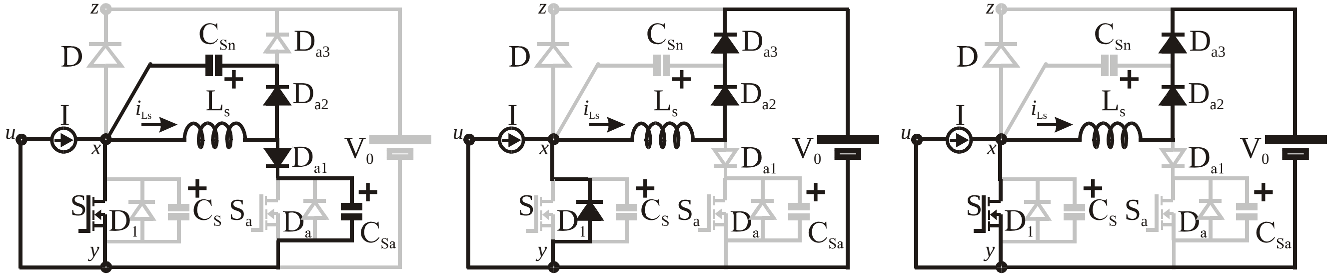
This mode ends when i_{Ls} reaches the value of current I.

$$t_1 - t_0 = I L_S / V_{ZY} \qquad (2)$$

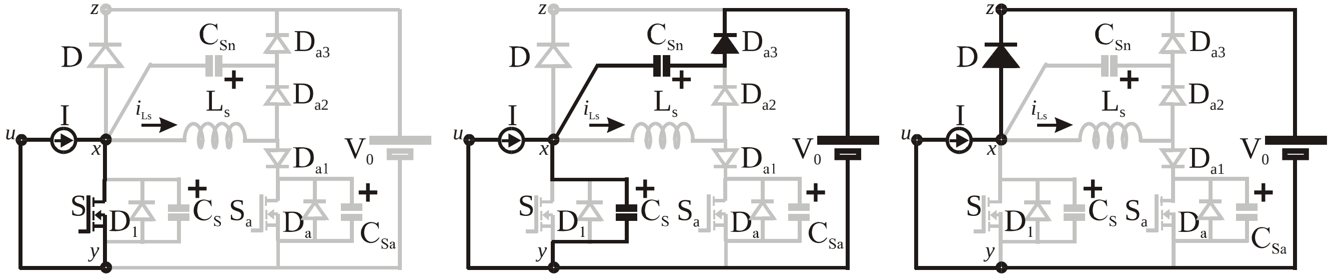
Mode 2 ($t_1 < t \leq t_2$)**:** At t_1 diode D turns off and the energy stored in C_S discharges through L_S in a resonant way. The resonant process is governed by the following expressions.



Mode 1 [t_0,t_1] Mode 2 [t_1,t_2] Mode 3 [t_2,t_3]



Mode 4 [t_3,t_4] Mode 5 [t_4,t_5] Mode 6 [t_5,t_6]



Mode 7 [t_6,t_7] Mode 8 [t_7,t_8] Mode 0 [t_9,t_0]

Figure 3. Operation Modes.

$$i_{Ls} = I + V_{ZY}\sin\left(\omega_S t\right)/Z_S \tag{3}$$

$$v_{Cs} = V_{ZY}\cos\left(\omega_S t\right) \tag{4}$$

Where, $\omega_S = 1/\sqrt{L_S C_S}$ and $Z_S = \sqrt{L_S/C_S}$.

This mode lasts until C_S to be completely discharged.

$$t_2 - t_1 = \pi\sqrt{L_S C_S}/2 \tag{5}$$

Mode 3 ($t_2<t\leq t_3$)**:** At t_2 main switch body-diode D_1 turns on. ZVS and ZCS conditions are ensured for main switch turn-on. This freewheeling interval should be as small as possible to minimize the auxiliary circuit conduction losses, however, it must last time enough to the gate source voltage signal turn S completely on.

Mode 4 ($t_3<t\leq t_4$)**:** At t_3 S_a is turned off, bypass diode D_{a2} is turned on and i_{Ls} resonates with the equivalent parallel capacitance comprised by C_{Sn} and C_{Sa}. As $C_{Sa} << C_{Sn}$, the dv/dt control is actually accomplished by C_{Sn}.

The resonant process is governed by the following expressions.

$$i_{Ls} = i_{Ls}\left(t_3\right)\cos\left(\omega_{eq} t\right) \tag{6}$$

$$v_{Csn} = Z_{eq} i_{Ls}\left(t_3\right)\sin\left(\omega_{eq} t\right) \tag{7}$$

Where, $\omega_{eq} = 1/\sqrt{L_S\left(C_{Sn} + C_{Sa}\right)}$ and $Z_{eq} = \sqrt{L_S/\left(C_{Sn} + C_{Sa}\right)}$.

In this mode, current I is diverted to main switch.

This mode lasts until v_{Csn} reaches V_{zy}.

$$t_4 - t_3 = \sin^{-1}\left(V_{ZY}/Z_{eq} i_{Ls}\left(t_3\right)\right)/\omega_{eq} \tag{8}$$

Mode 5 ($t_4<t\leq t_5$)**:** At t_4 bypass diode D_{a3} turns on and voltage across C_{Sn} and C_{Sa} is clamped at V_{zy}. In this mode i_{Ls} decreases linearly with the following ratio.

$$i_{Ls} = i_{Ls}\left(t_3\right) - V_{ZY} t/L_S \tag{9}$$

This mode ends when main switch body-diode turns off.

$$t_5 - t_4 = \left(i_{Ls}\left(t_3\right) - I\right) L_S/V_{ZY} \tag{10}$$

Mode 6 ($t_5<t\leq t_6$)**:** In this mode, i_{Ls} continues to decrease linearly with the ratio defined by (9). This mode lasts until i_{Ls} reaches zero.

$$t_6 - t_5 = I L_S/V_{ZY} \tag{11}$$

Mode 7 ($t_6<t\leq t_7$)**:** In this mode, current I flows through S and converter operates as its PWM counterpart. The converter PWM modulation governs the duration of this mode.

Mode 8 ($t_7<t\leq t_8$)**:** At t_7 main switch is turned off and voltage across its terminals increases linearly with the ratio defined below.

$$v_{Cs} = \left(I/\left(C_{Sn} + C_S\right)\right)t \tag{12}$$

As $C_S << C_{Sn}$, the dv/dt control is actually performed by C_{Sn}

This mode ends when v_{Cs} reaches V_{ZY}.

$$t_8 - t_7 = \left(C_{Sn} + C_S\right)V_{ZY}/I \tag{13}$$

Mode 9 ($t_8<t\leq t_0$)**:** At t_8, v_{Cs} reaches V_{ZY} and diode D turns on. In this mode, current I flows through D.

The main theoretical waveforms are shown in Fig. 4.

3 IMPROVED SNUBBER DESIGN

In conventional design guidelines (Yaakov e*t al.*, 1995; Liu *et al.*, 2000), auxiliary elements L_S and C_S are defined as a function of the current stresses on auxiliary switch, given by k_I,

$$k_I = \left(1 + \left(V_{ZY}/Z_S\, I\right)\right) \tag{14}$$

and the total ZVS time, given by t_{ZVS},

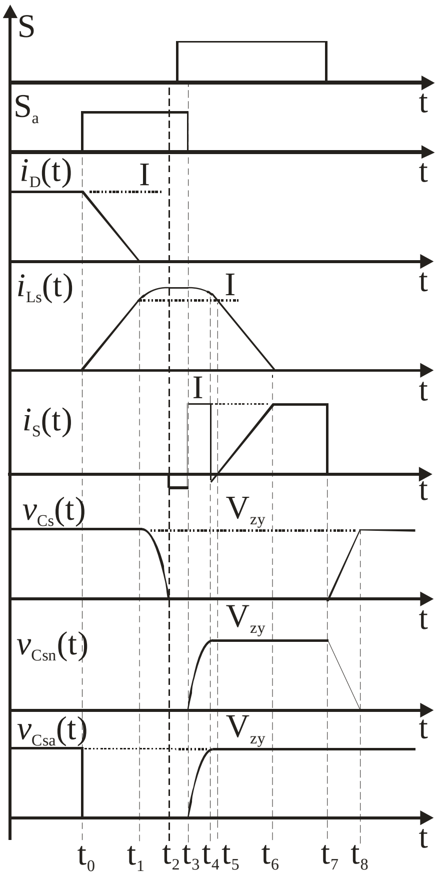


Figure 4. Main Theoretical Waveforms.

$$t_{ZVS} = IL_S/V_{ZY} + \pi\sqrt{L_S C_S}\big/2 \qquad (15)$$

Solving (14) and (15) for L_S and C_S the following expressions can be found,

$$L_S = V_{ZY} t_{ZVS}\big/ I\left(1+\pi\left(k_I-1\right)/2\right) \qquad (16)$$

$$C_S = It_{ZVS}\left(k_I-1\right)^2\big/V_{ZY}\left(1+\pi\left(k_I-1\right)/2\right) \qquad (17)$$

Where k_I is directly related to the conduction losses and are chosen to be in a range between 1.3 and 1.5 times of current I and t_{ZVS} is related to the Minimum and maximum duty-cycle. For DC-DC converter t_{ZVS} is in a range of 10% to 15% of converter operation period. On the other hand, in PFC applications it is significantly reduced to a range of 2% to 3% of the converter operation period.

The auxiliary capacitor C_{Sn} is chosen to assure the time conditions given by t_{ZVS} or to ensure turn-off smoothness for S_a.

The ZVT DC-DC PWM converter with SAAS has a unique characteristic that consist of the presence of a turn-off snubber C_{Sn} across the auxiliary inductor L_S. By a proper choice of C_{Sn} it can also smooth the main switch turn-off commutation process. This way, main switch snubber capacitor can be as small as possible without penalizing the turn-off losses.

As the energy stored in C_{Sn} is regenerated to the output without circulating through L_S, C_{Sn} can be made large enough to ensure low switching losses for both, main and auxiliary switch with no additional conduction losses.

To ensure snubber operation for S and S_a, C_{Sn} must verify the following expression.

$$C_{Sn} \le L_S\left(I+\left(V_{ZY}/Z_S\right)\right)^2\big/V_{ZY}{}^2 \qquad (18)$$

Expression above is graphically represented in the state-plane $Z_{Sn}i_{Ls}$ x v_{Csn}, shown in Fig. 5.

Once that (18) is true, C_{Sn} can be chosen to optimize the switching conditions of main switch during its turn-off by the expression below,

$$C_{Sn} \ge I\big/\left(dv_{Sa}/dt_{MAX}\right) \qquad (19)$$

In order to ensure low current stresses and conduction losses through the auxiliary circuit snubber capacitors C_S and C_{Sa} can be made the smallest possible. This way, they are considered as the intrinsic output capacitances (C_{oss}) of each switch, respectively.

$$C_S = C_{oss}(S) \qquad (20)$$

$$C_{Sa} = C_{oss}(S_a) \qquad (21)$$

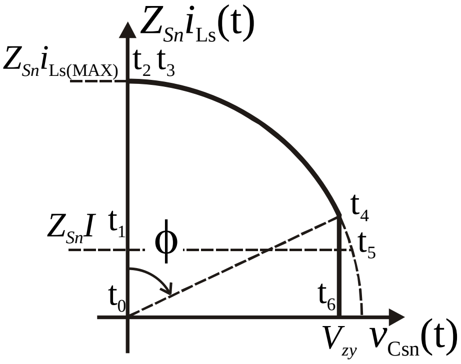


Figure 5. Turn-off Snubber Condition given by Expression (18).

As C_S and C_{Sa} guarantee low conduction losses, inductor L_S can be chosen to optimize the turn-off conditions of the main diode D. Therefore,

$$L_S \ge V_{ZY}\big/\left(di_D/dt_{MAX}\right) \qquad (22)$$

4 COMPARATIVE ANALYSIS

To evaluate the gains obtained by the proposed snubber design optimization, the converter with SAAS presented in (Yaakov *et al.*, 1995) is implemented using both design guidelines, the original design guidelines provided in (Yaakov *et al.*, 1995) and the design guidelines described in previous section (Section 3). Table 1 gives the converter specifications.

4.1 Design guidelines from reference (Yaakov et al., 1995)

By (Yaakov *et al.*, 1995) the resonant auxiliary elements are calculated using expressions (16), (17) and (23).

$$C_{Sn} = \left(I+V_{ZY}/Z_S\right)\big/\left(dv_{Sa}/dt_{MAX}\right) \qquad (23)$$

As L_S and C_S are function of k_I and t_{ZVS}, expressions (16) and (17) are depicted in Fig. 6 for a range of values of k_I (1.0 to 2.0) and t_{ZVS} (2% to 20%T), where the converter operation period T is given by $T = 1\big/f_s$. From (Yaakov *et al.*, 1995) typical values of k_I lie in the range of 1.3 and 1.5, whilst t_{ZVS} is in the range of 2% to 3% of T for Power Factor Correction (PFC) applications (Bazinet and O'Connor, 1994). and in the range of 10% to 15% for DC-DC applications (Zhu and Ding, 1999). For comparative purposes, k_I is chosen equal to 1.4 and t_{ZVS} equal to 10% T. By means of Fig. 6, L_S and C_S are found as, 35μH and 1.8nF, respectively. By expression (23), C_{Sn} is calculated equal to 2.8nF.

Table 1. Specifications of power converter prototypes.

Component	Parameter	
	ZVT PWM converter with snubber assisted auxiliary switch.	**True-PWM ZVS pole boost converter.**
V_i	150 V	150 V
V_0	400 V	400 V
P_0	1.0 kW	1.0 kW
f_S	100 kHz	100 kHz
L	0.9 mH	0.9 mH
C	150 uF	150 uF
S	IRFP450	IRFP450
S_a	IRF840	HGTP3N60C3D
D	MUR1560	MUR1560
D_{a1}, D_{a2},D_{a3}	RHR870	MUR1560

4.2 Design guidelines from Section III

Once that condition given by expression (18) is ensured, the auxiliary elements are calculated by expressions (19) and (22), as L_S= 4μH, C_{Sn}= 2.7nF (IRF840) and C_S is the output capacitance of the MOSFET (0.4nF) itself. Due to the non-linear characteristic of the MOSFET output capacitance (C_{oss}) it is estimated as two or three times smaller than the value presented by the data sheet (C_{oss}= 310pF, V_{DS}= 25V) (International Rectifiers, Application note), resulting in a value for C_S of about 155pF. Therefore, $Z_S = \sqrt{L_S/C_S} \approx 160.6\Omega$ ·

5 EXPERIMENTAL RESULTS

In order to compare the efficiency gain of the proposed optimized snubber design, the performance of the ZVT DC-DC PWM boost converter with SAAS (Streit and Tollik, 1991; Yaakov *et al.*, 1995; Liu *et al.*, 2000; Kim *et al.*, 2000; Menegáz *et al.*, 1999) was evaluated on a 1 kW, 100 kHz laboratory prototype. The main converter parameters are summarized in Table 2. Two sets of auxiliary circuit elements were built. For the first set, the elements were specified following the design guidelines given by (Yaakov *et al.*, 1995) and presented in Section 4.1, Fig. 7(a). For the second set, the elements were specified following the optimized snubber design presented in Section 4.2, Fig. 7(b).

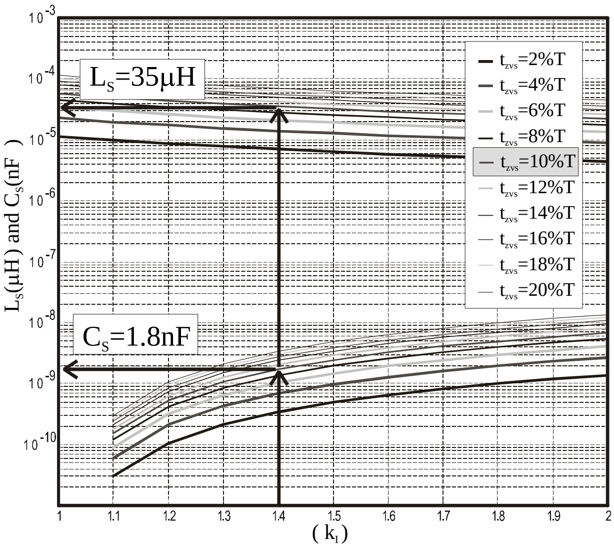
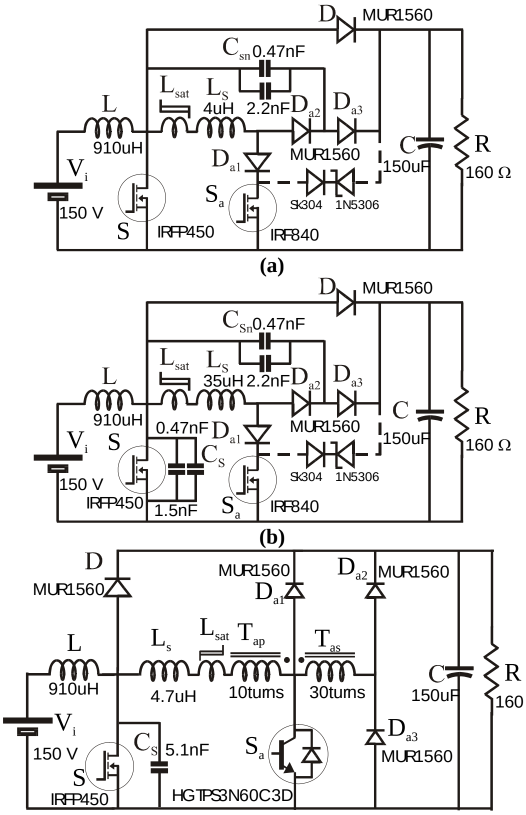


Figure 6. Representation of Expressions (16) and (17).

Moreover, a ZVT PWM boost converter with auxiliary DC voltage source, Fig. 7(c), was also compared. The parameters of this topology are given in Table 2. To reduce



(a)

(b)

(c)

Figure 7. Diagrams of Implemented Prototypes. ZVT PWM boost converter with SAAS: (a) By Snubber Improved Design; (b) By Design of (Yaakov et al., 1995) (c) True-PWM ZVS Pole Boost Converter (Martins et al., 1993).

Table 2. Auxiliary Circuit Parameters.

Component	Parameter		
	ZVT PWM converter with SAAS.		**True PWM ZVS pole boost converter, ref. [5].**
	Proposed	**Ref [16].**	
L_S	4μH	35μH	3.7μF(+L $_k$=1uF)
C_s	0.4nF	1.8nF	5.1 nF
C_{Sn}	2.7nF	2.8nF	-----
F. Core	----	----	EE-30/14
N. of Turns	----	----	10/30

the auxiliary semiconductors and coupled inductors parasitic capacitance effects, a saturable inductor, implemented with 8 turns on a Toshiba “spike killer” core (SA 14x8x4.5) was used in series with L_S.

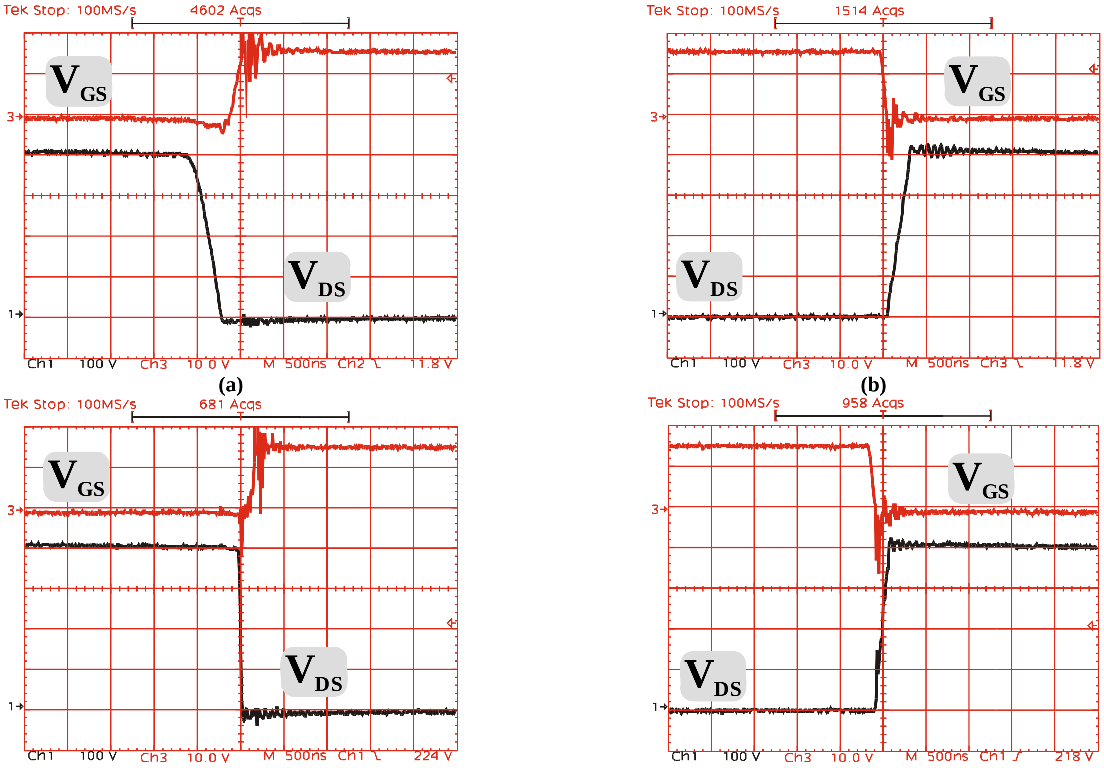
Fig. 8 shows the most relevant experimental waveforms obtained from the ZVT PWM boost converters with SAAS prototypes. It can be seen by the waveforms of voltage across the main switches that soft-switching conditions are achieved for main switch turn-on and turn-off processes, Fig. 8(a) and 8(c) for the original design guidelines and in Fig. 8(b) and 8(d) for the presented improved design guidelines, respectively.

In Fig. 9 it can be seen that the maximum current through L_S is slightly lower in the original design guidelines Fig. 9(a) than that in the presented improved design guidelines Fig. 9(b). However, the commutation time is higher in the original design guidelines, Fig. 9(a), which ensures low conductions losses to the presented improved design guidelines. In Fig. 9 it also can be seen that auxiliary switch turn-off is smooth due to the presence of C_{Sn}. Actually, a perfect voltage turn-off of main switch cannot be achieved due to the voltage drop across C_{Sn} occurred at instant t_6, when the reverse recovery of diodes D_{a2} and D_{a3} take place. Thus, turn-off losses of main switch are function of L_S and input current I.

Fig. 10 shows the waveforms in the snubber elements, L_S and C_{Sn}, where the above mentioned voltage drop can be seen.

By Fig. 11 it can be seen that, at full load, the efficiency of the converter designed by the improved snubber design (circles) is about 0.5% higher and the average efficiency gain for the entire output range is higher than 0.5% compared to the original design (triangles). Besides, the improved snubber design also achieved higher efficiency for about 80% of entire load range compared to a True PWM ZVS pole boost converter (squares). As a result of the auxiliary circuit lower conduction, the ZVT PWM with SAAS with the proposed design presents higher efficiency in light and medium load condictions. This feature is offset by the turn-off losses of main switch, which are increased in high load conditions due to reverse recovery of auxiliary diodes.

To overcome this problem it is required to consider not only the main diode (D) di/dt requirements but also the auxiliary diodes di/dt to compute the auxiliary inductor L_S. However, a trade-off between the auxiliary circuit conduction losses and turn-off losses of main switch should be defined and adopted to calculate L_S. With this trade-off the efficiency may be even improved.



(a) (b) (c) (d)

Figure 8. Main Switch Experimental Waveforms. (a) and (b) For Original Design Guidelines; (c) and (d) For Presented Improved Design Guidelines. Scales: V_{GS}: 10 V/div; V_{DS}: 100 V/div; Time – 500 ns/div.

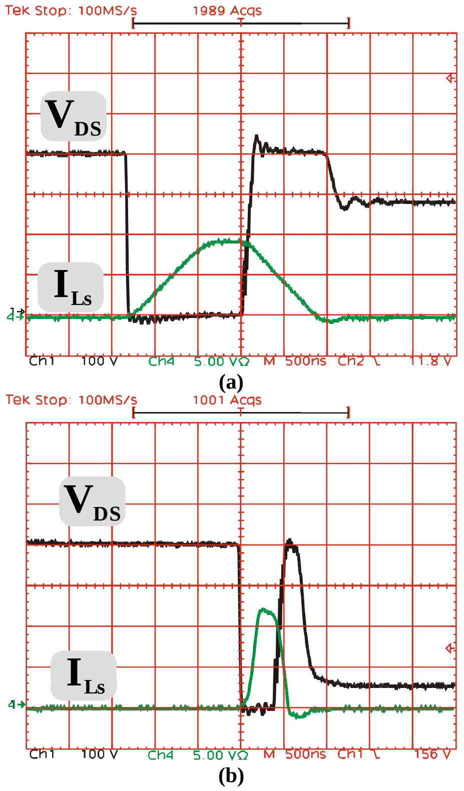


Figure 9. Auxiliary Switch Experimental Waveforms. (a) For Original Design Guidelines; (b) For Presented Improved Design Guidelines.
Scales: I_{Ls}: 5 A/div; V_{Csn}: 100 V/div; Time – 500 ns/div.

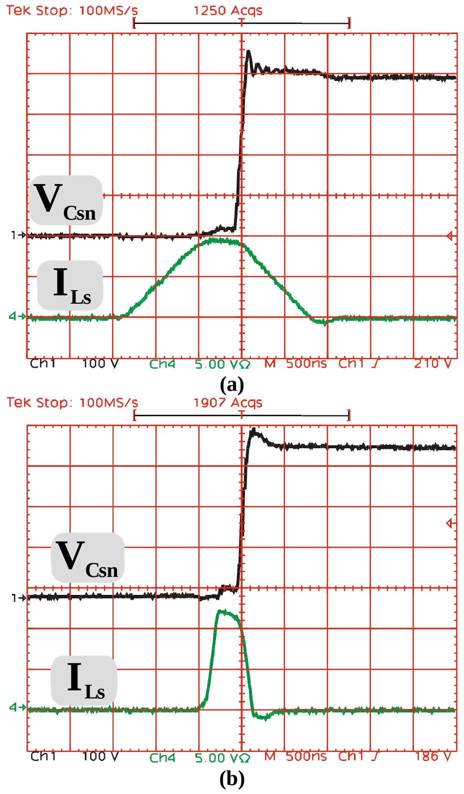


Figure 10. Snubber Elements Experimental Waveforms. (a) For Original Design Guidelines; (b) For Presented Improved Design Guidelines.
Scales: I_{Ls}: 5 A/div; V_{Csn}: 100 V/div; Time – 500 ns/div.

6 CONCLUSION

This paper presented an improved design to calculate the auxiliary elements of the ZVT DC-DC PWM converters with snubber assisted auxiliary switch. The presented design guidelines are based on the unique location of the turn-off snubber capacitor shared by the active switches. As the snubber energy does not circulate through auxiliary inductor, a reduction of the auxiliary circuit conduction losses can be achieved. As a result, converter efficiency can be improved.

Theoretical analysis is confirmed by the comparison of experimental results obtained from two prototypes designed by the presented improved design guidelines and by the original ones (Yaakov *et al.*, 1995). The results show an efficiency gain higher than 0.5% for entire output power range.

In addition, experimental results also have shown that with the improved design the ZVT PWM converters with SAAS can be competitive with ZVT PWM converters with constant auxiliary voltage source (True PWM ZVS pole) in a large load range, which makes the ZVT with SAAS converter a strong candidate for PFC applications. On the other hand, the ZVT with SAAS converter presented smaller efficiency at full-load (20%), its smaller component count and design simplicity still make it competitive, when compared to the True PWM ZVS pole converter.

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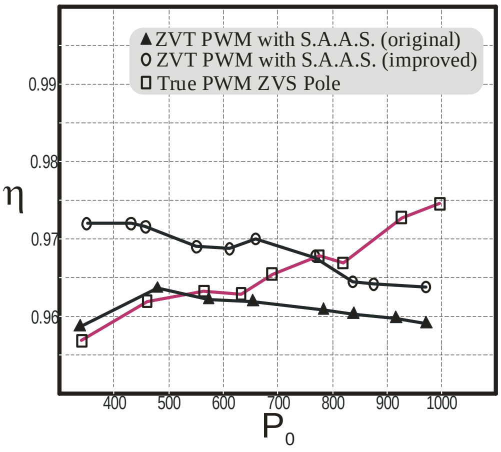

Figure 11. Efficiency Curves.

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