# EFFECTIVE LIMITATION OF LINE FAULT CURRENTS BY MEANS OF THE SERIES-CONNECTED VSC-BASED FACTS DEVICES

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## ABSTRACT

In this paper, the nearly instantaneous response of the series-connected VSC-based FACTS controllers when used to limit possible fault currents in a compensated line, will be presented. The effectiveness of both FACTS controllers (SSSC and UPFC) towards this system condition was investigated exploring the series voltage effect upon the line. Moreover, it will be shown that the UPFC shunt converter can also contribute to the reduction of such fault currents. The short-circuit current limitation strategy presented herein showed that aside of the power flow control and voltage support commonly carried out by the SSSC and the UPFC, they could also perform this additional functionality, thus offering a useful tool for the protection of the line in which these devices are installed.

**KEYWORDS**: FACTS, Short-circuit, SSSC, UPFC, VSC.

## 1   INTRODUCTION

Short-circuit current limiters could be implemented because of two reasons: to reduce the stress within the network and/or to limit the stress over a certain asset, as it might be the case of the series-connected converters referred in this paper. Modern power systems are built with a high degree of flexibility so that, ideally, a minimum part of the system would be interrupted during the fault period. Presently, investigations are being carried out to study the coordination of the distance protection and the line's apparent impedance variation of those lines implemented with FACTS (Flexible AC Transmission Systems) devices, mainly those connected in series with the line. Also, the fault clearing time is not instantaneous for it depends on the operating time imposed to the overcurrent relays and the circuit-breaker's tripping time.

The series-connected VSC (Voltage-Sourced Inverter) based FACTS devices referred in this paper, are: the SSSC (Static Synchronous Series Compensator) and the UPFC (Unified Power Flow Controller). These devices have nearly instantaneous responses and enable to control more effectively the power flow on the lines where they are installed. As it is known, both the SSSC and the UPFC basically inject a nearly sinusoidal voltage ($V_{se}$) in series with the line. The voltage ($V_q$) of the former is in quadrature at an angle $\pm 90°$ with respect to the line current. The latter also injects a series voltage to the line, but its phase angle can freely rotate along the 360 degrees describing a circle whose maximum radius is equal to $V_{se}^{max}$.

Both VSC-based compensators use a DC capacitor as a source for the waveform generation. The presence of transients in the compensated line (short-circuits, etc) causes the

DC voltage in both devices to fluctuate. This fluctuation is proportional to the line current and to the injected voltage itself. The UPFC shunt VSC helps to cope with this problem by controlling the DC voltage. In other words, the shunt converter damps these fluctuations and keeps the DC voltage almost constant. In this work, it will be considered that the referred fluctuations do not alter significantly the compensation characteristic of the devices aimed to limit the fault currents.

In recent years, some other FACTS devices have emerged for developing similar functions. It is the case of the SCCL (Short Circuit Current Limiter) which has shown to be effective for this specific purpose; it is also the case of the TCSC (Thyristor Controlled Series Capacitor) as reported by Moschakis *et alii* (2003). The fault limitation approach presented here may not be cheaper nor simpler than other type of short-circuit current limitation strategies, but it does explore this attractive tool and additional functionality of the series-connected VSC-based FACTS controllers.

In this article, it will be presented the basis to manipulate the series voltage injected from both the SSSC and the UPFC, so as to get the maximum effect whilst limiting short-circuit currents. Further, it will be shown that the UPFC shunt converter can also contribute to the reduction of fault currents by forcing the bus voltage at its point of connection, therefore at the fault point, to reduce its magnitude.

## 2  FAULT CURRENT LIMITATION

It is well established that the short-circuit current levels in a certain network increases proportionally with the addition of lines and new generation. This may jeopardize the transformation and transmission assets in existing power systems, for the short-circuit current rating of such equipment, if not modified and updated or even replaced, will be exceeded. Under these circumstances, the fault current limitation offered by modern controllers, characterized by their nearly instantaneous responses, may become crucial in diminishing such large currents. Hence the interest for analyzing the topic discussed in this paper.

The fault current limitation based on impedance control is a well known subject. For three-phase faults, the inclusion of limiting reactors is a common method whereas for phase-to-ground faults, the use of grounding devices and modifications of the zero sequence impedance, are usual practices. However, information on the use and application of the FACTS devices for short-circuit limitation is somewhat scarce. In a study presented by Salem and Sood (2005) a PWM (Pulse Width Modulation) VSC-based SSSC built in the EMTP RV program, is presented. Although in that paper it i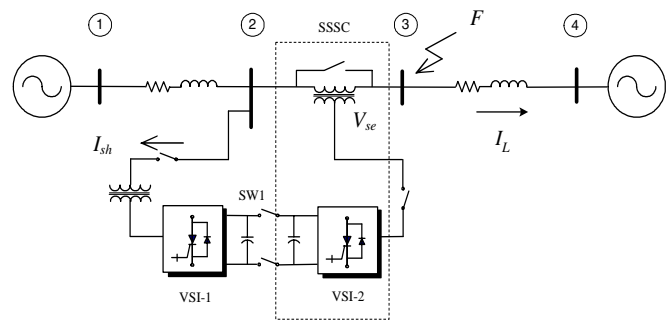s also addressed the fault current limitation as an outstanding byproduct of this device, the authors mainly emphasized aspects such as the inverter's waveform generation technique and the control system of both the converter itself and the quadrature voltage injected onto the line. The scope of our paper, unlike the one mentioned, emphasizes the effect and contribution of the FACTS devices herein referred for limiting fault currents. Still, whenever applicable details of either device implemented in the ATP program, will be included.



Figure 1: Series-connected VSC-based devices for fault limiting analysis

The respective leakage reactance of the series coupling transformer reduces, although to a smaller extent, the short-circuit current that may be originated in the compensated line (passive fault limitation). Thus, if an emulated reactance of greater value is inserted into the line, in an almost instantaneous way, the stress of the compensated line as a result of the fault, can be limited to a considerable degree.

The fault limitation strategy using FACTS devices was first explored by Duangkamol *et alii* (2000) followed by Takeshita *et alii* (2002). Here, we will further explore this topic and will show the contribution of the UPFC shunt and series converters towards this system condition. The system depicted in Figure 1, will be used to analyze and simulate the referred fault current limitation strategy. The simple connection of the switch, SW1, makes of the stand-alone operating VSCs (SSSC and STATCOM) to complete the UPFC arrangement. Typically, both SSSC and UPFC devices are mainly used for power flow control (Gyugyi, 1991; Papic *et alii*, 1997; Huang *et alii*, 2000; Vasquez-Arnez *et alii*, 2002 and Sen, 1998). An additional function of the shunt VSC being the line voltage support.

Under no fault conditions, the voltage ($V_{se}$) and its respective angle ($\theta_{se}$), will give rise to a family of curves like those depicted in Figure 2. To obtain these curves both series and shunt converters were regarded as ideal sources operating at fundamental frequency (Uzunovic *et alii*, 1998; Yu *et alii*, 1996). Also, the resistive component in each transmission line was neglected and both sending and receiving-end ideal sources were set to 1.0 pu at angles 0° and -30°, respectively.

The referred steady-state curves show the extent in which the line's active and reactive power in the receiving-end, can be controlled. Notice, for the forthcoming analysis, the values of the series angle ($\theta_{se}$) for which $P$ and $Q$ are substantially compensated.

The condition to achieve the short-circuit current limitation is to keep the voltage $V_{se}$ ($V_q$ in the SSSC configuration) injected in the line even during the fault period. Recall that for the SSSC case (Sen, 1998), the relation of the quadrature series voltage, $V_q$, over the line current will be seen by the system as a compensating reactance, $X_C$, which emulates an inductive (or capacitive) reactance in series with the line $V_q/I_L = \pm j X_C$. As for the UPFC, the relation between the series voltage, $V_{se}$, and the line current can be seen as a positive (negative) resistance ($\pm R$) and a positive (negative) reactance ($\pm jX$) in series with the line (Gyugyi, 1991). Although this concept can be used to explain the fault current limiting effect, we will prefer to analyze such current control from the series injected voltage viewpoint.

The idea behind the fault-current limitation concept (for three-phase and phase-to-ground faults) is to minimize the voltage at the fault point through the action of the series voltage, $V_{se}$. This, in fact, is an extension of the Thevenin's pre-fault voltage concept at the fault point. For the case of a three-phase fault occurring at bus 3 (Figure 3), it can be seen the contributions of the two independent loops L (left) and R (right) to the fault point. In fact, the series voltage will reduce the current contribution from the left AC system ($E_1$).

This reduction will be more effective when the UPFC injects positive sequence voltages in opposition to the left equivalent source, which can be estimated in each operative condition. If it is intended to minimize the total current at the fault point, the series voltage injected must be in opposition to the pre-fault voltage at the fault point. As the voltage along the line has a smooth behavior, it is not difficult to set values to cover some other cases of faults along the compensated line.

## 3 FAULT CURRENT LIMITATION ANALYSIS

Initially, it will be defined the left and right equivalent impedances, from the fault point up to each AC source, as $Z_L$ and $Z_R$, respectively. For a phase-to-ground fault, which is the case more likely to occur, the sequence diagrams are sequentially connected, therefore, to minimize the current contributions to the fault, a more careful analysis must be performed. Such an analysis can be done through phase or sequence components.

Thus, regarding the fault point considered in Figure 3, which can be located at any point along the line $Z_2$, and with the
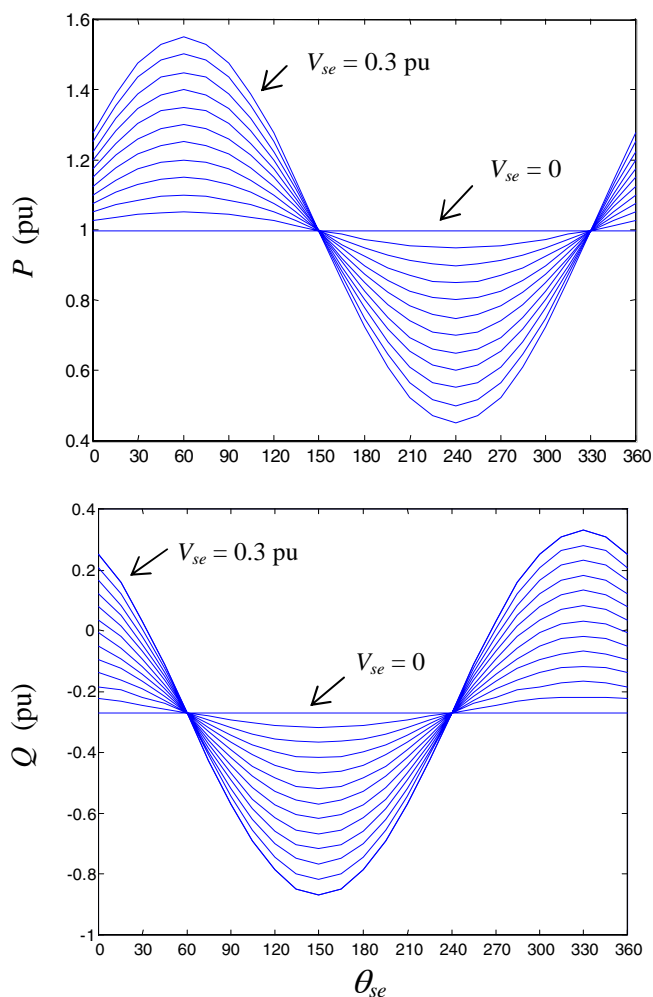


Figure 2: Steady-state active and reactive power flow control ($0 \le \theta_{se} \le 360°$) at the receiving end
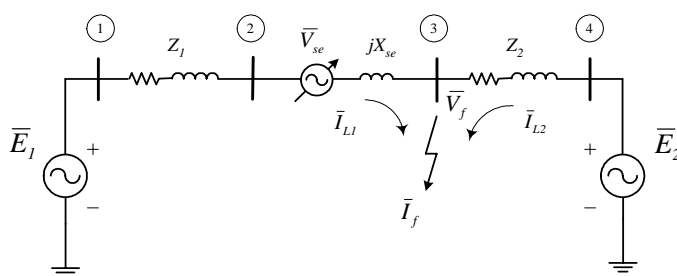


Figure 3: Series VSC converter seen as a fundamental frequency source for fault analysis

term $X_{se}$ included within the equivalent impedance $Z_L$ (left-side), it can be established that:

$$[E_1'] = [E_1] + [V_{se}] \qquad (1)$$

Under the absence of the fault, the line current in the system will be,

$$[I_L] = [Z_L + Z_R]^{-1}[E_1' - E_2] \qquad (2)$$

The pre-fault voltage at bus 3 can be expressed as:

$$[V_3] = [E_2] + [Z_R][I_L] \qquad (3)$$

Substituting (2) into (3) and calling $M$ the matrix that represents the voltage divider, yields:

$$[V_3] = ([I] - [M])[E_2] + [M][E_1] + [M][V_{se}] \qquad (4)$$

where, $[I]$ represents the identity matrix. Also,

$$[M] = [Z_R][Z_L + Z_R]^{-1} \qquad (5)$$

In order to simplify (4), the first two terms (i.e. those affected by $E_1$, $E_2$ without the effect of $V_{se}$) will be named as $V_{uf}$ (uncompensated fault voltage), whereas the last term will be designated as $V_{sc}$ (series compensating voltage at the fault point $F$). Thus, the compensated fault voltage ($V_f$) in (4), former $V_3$, becomes:

$$[V_f] = [V_{uf}] + [M][V_{se}] \qquad (6)$$

To minimize $V_f$, the compensation term $[M][V_{se}]$ has to be in opposition to $V_{uf}$, with the series voltage ($V_{se}$) being inserted at its maximum possible magnitude during the fault period.

The above equations and analysis correspond to a generic case of a tripolar fault. For the case of a phase-to-ground fault, some other aspects, such as the effect of the healthy phases should also be considered. This aspect is to be clarified (i.e. to observe whether the coupling effect of the unaffected phases can contribute or not to the fault current limitation). In the analyzed case only the inductive effect of the unaffected phases, will be considered. So, if the product of the resulting impedance matrices in (5) were renamed as that shown in (7) where to simplify the analysis transposed lines are considered, we will have:

$$[M] = \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \qquad (7)$$

Factors $\alpha$, $\beta$ are dependent on the equivalent impedances $Z_L$ and $Z_R$ and on the zero and positive sequence values which define the coupling effect between phases. The substitution of (7) into (6), yields:

$$\begin{bmatrix} \bar{V}_{fa} \\ \bar{V}_{fb} \\ \bar{V}_{fc} \end{bmatrix} = \begin{bmatrix} \bar{V}_{ufa} \\ \bar{V}_{ufb} \\ \bar{V}_{ufc} \end{bmatrix} + \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \begin{bmatrix} \bar{V}_{sea} \\ \bar{V}_{seb} \\ \bar{V}_{sec} \end{bmatrix} \qquad (8)$$

For instance, the corresponding terms affecting the fault point at phase $a$, are:

$$\bar{V}_{fa} = \bar{V}_{ufa} + \alpha \bar{V}_{sea} + \beta \left( \bar{V}_{seb} + \bar{V}_{sec} \right) \qquad (9)$$

For the case of the system depicted in Figure 3, if $Z_{L1}$=0.25, $Z_{L0}$=0.545, $Z_{R1}$=0.25, $Z_{R0}$=0.8695, then, the values of the factors $\alpha$ and $\beta$ computed, will be: $\alpha$=0.538 and $\beta$=0.038. Thus, according to (9) two different strategies can be adopted for analyzing the effect of the voltage $V_{se}$.

a) Regarding the positive sequence in the three phases $(\bar{V}_{sea} + \bar{V}_{seb} + \bar{V}_{sec} = 0)$, then, the voltage $V_{se}$ at phase $a$ will be:

$$\bar{V}_{fa} = \bar{V}_{ufa} + (\alpha - \beta)\bar{V}_{sea} \qquad (10)$$

in this case, the healthy phases can introduce a deleterious effect on the voltage at the fault point.

b) With the introduction of the zero sequence voltage $(\bar{V}_{sea} = \bar{V}_{seb} = \bar{V}_{sec})$ equation (9) becomes:

$$\bar{V}_{fa} = \bar{V}_{ufa} + (\alpha + 2\beta)\bar{V}_{sea} \qquad (11)$$

The voltage control is improved compared to the previous positive sequence voltage compensation.

In order to analyze the contribution of the currents to the fault point, it will also be examined the sequence impedance diagrams depicted in Figure 4, in which:

$\bar{I}_1, \bar{I}_2, \bar{I}_0$ : sequence components of the fault current.

$\bar{I}_{L1}, \bar{I}_{L2}, \bar{I}_{L0}$ : sequence components of the left-side equivalent contribution.

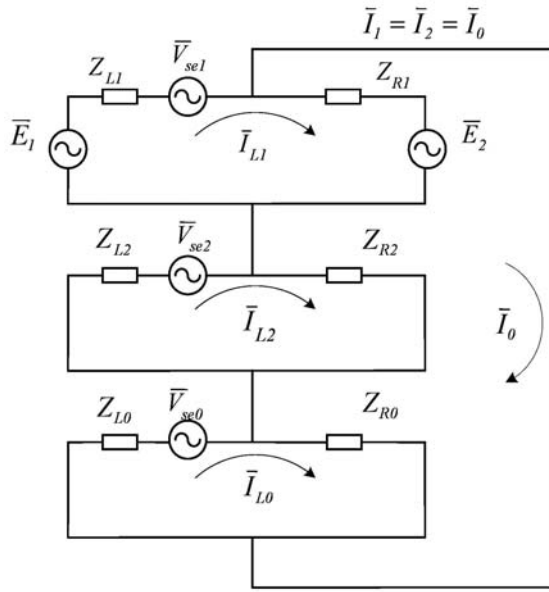The loop equations from the diagram shown in Figure 4 are:

Figure 4: Phase-to-ground fault: equivalent sequence diagrams

$$
\begin{bmatrix} \bar{E}_1 + \bar{V}_{se1} - \bar{E}_2 \\ \bar{V}_{se2} \\ \bar{V}_{se0} \\ \bar{E}_2 \end{bmatrix} = \begin{bmatrix} (Z_{L1} + Z_{R1}) & 0 \\ 0 & (Z_{L2} + Z_{R2}) \\ 0 & 0 \\ -Z_{R1} & -Z_{R2} \end{bmatrix}
$$

$$
\begin{bmatrix} 0 & -Z_{R1} \\ 0 & -Z_{R2} \\ (Z_{L0} + Z_{R0}) & -Z_{R0} \\ -Z_{R0} & (Z_{R1} + Z_{R2} + Z_{R0}) \end{bmatrix} \begin{bmatrix} \bar{I}_{L1} \\ \bar{I}_{L2} \\ \bar{I}_{L0} \\ \bar{I}_0 \end{bmatrix} \quad (12)
$$

or, in its compact form:

$$
[E] = [Z][I] \quad (13)
$$

Voltages $\bar{V}_{se1}$, $\bar{V}_{se2}$ and $\bar{V}_{se0}$ are the sequence components of the series voltage injected by the UPFC. Recalling also that:

$$
[I] = [Y][E] \quad (14)
$$

Where: $[Y] = [Z]^{-1}$, then the zero sequence fault current can be obtained through (15):

$$
\bar{I}_0 = Y_{41}\bar{E}_1 + (Y_{41} - Y_{44})\bar{E}_2 + (Y_{41}\bar{V}_{se1} + Y_{42}\bar{V}_{se2} + Y_{43}\bar{V}_{se0}) \quad (15)
$$

The first two terms of the second member in (15) represent the fault current without the presence of the series voltages. The remaining terms representing the contribution of the series voltage. Obviously, the fault current can be obtained through:

$$
\bar{I}_f = 3\bar{I}_0 \quad (16)
$$

Equation (14), shown some lines above, is in accordance to the concept of minimizing the pre-fault voltage at the fault point and it shows the most significant effect of applying positive or zero sequence voltage by analyzing the admittance matrix terms with positions $Y_{41}$ or $Y_{43}$, similarly to the analysis developed in (10) and (11). Let's now obtain the left-side equivalent contribution to the fault current.

$$
\bar{I}_L = (\bar{I}_{L1} + \bar{I}_{L2} + \bar{I}_{L0}) \quad (17)
$$

This current is obtained through the addition of the first three rows in (14) in which the equivalent admittances are defined as:

$$
Y_j = \sum_{i=1}^{3} Y_{ij} \quad (18)
$$

where, $Y_j$ is composed by the sum of the first three elements of each column.

A similar expression to that shown in (14) can be developed for the left-side current contribution ($I_{LC}$) to the fault current. That is:

$$
\bar{I}_{LC} = \underbrace{Y_1\bar{E}_1 + (Y_1 - Y_4)\bar{E}_2}_{\bar{I}_{LU}(\text{uncompensated})} + \underbrace{Y_1\bar{V}_{se1} + Y_2\bar{V}_{se2} + Y_3\bar{V}_{se0}}_{\bar{I}_{LSC}(\text{contribution of } V_{se})} \quad (19)
$$

Again, the first two terms of the second member in (19) refers to the fault current contribution without the series voltage ($\bar{I}_{LU}$), whereas the remaining terms refer to the series voltage contribution ($\bar{I}_{LSC}$). In order to minimize the contribution to the total fault current, $\bar{I}_{LSC}$ must be in opposition to $\bar{I}_{LU}$. The best strategy for applying either the positive or zero sequence voltage from $\bar{V}_{se}$, for each specific system, must be chosen analyzing the elements $Y_1$ and $Y_3$ defined in (18). For example, using the parameters previously given, it can be obtained the respective Y matrix:

$$Y = -j \begin{bmatrix} \boxed{\begin{matrix} 0.0615 & 0.018 \\ 0.018 & 0.0615 \\ 0.034 & 0.034 \end{matrix}} & \boxed{\begin{matrix} 0.034 \\ 0.034 \\ 0.0875 \end{matrix}} & \begin{matrix} 0.0361 \\ 0.0361 \\ 0.0679 \end{matrix} \\ 0.0361 & 0.0361 & 0.0679 & 0.0722 \end{bmatrix}$$

$$Y_1 \qquad\qquad\qquad Y_3$$

$$(20)$$

For this case, $Y_1$=-j0.1135 pu and $Y_3$=-j0.1554 pu, thus, the values computed for the currents in (19) result in: $\bar{I}_{LU}$=15.46∠-95.56°pu, $\bar{I}_{LSC}$=5.25∠87°pu, $\bar{I}_{LC}$=10.22∠-96.87° pu. For this particular system, the zero sequence application of the series voltage, $\bar{V}_{se0}$, becomes more effective to reduce the left equivalent contribution to the fault current. Finally, with the sequence components it can also be analyzed the total fault current in (16). As $|Y_{43}| > |Y_{41}|$, the zero sequence voltage $\bar{V}_{se0}$ is again more effective for the total fault current reduction, this being in agreement with our previous analysis performed with phase components.

## 3.1 UPFC MODEL AND IMPLEMENTATION

In this section, it will be presented the main aspects related to the UPFC implementation in the ATP program. In order to generate the waveforms in each VSC, it was used the Harmonic Neutralized (HN) technique which consists in the series connection of all the wye connected secondary windings of the transformers within the magnetic circuit. In this way, the equivalent output waveform, containing 12, 24 or 48 pulses, will be composed by the sum of all the individual 2-level or 3-level inverters, depending on the type of configuration used. So as to generate the desired waveforms, the phase-shift among the inverters implemented must be properly set up. The four VSC-based inverters depicted in Figure 5, upon which was built our model, make use of this technique using common Δ-Y transformers as the magnetic interface between the VSCs and the AC system. A more detailed description on the waveform generation using this technique can be found in the reference authored by Sen *et alii* (1998).

The control sequence followed by the UPFC shunt current ($I_{sh}$) and the series voltage ($V_{se}$) along with their associate variables, are shown in Figures 6(a) and 6(b), respectively. The shunt controller adjusts dynamically the phase angle between the VSC-1 and bus $V_2$ in order to generate or absorb MVArs at the connection point. The series VSC operates similarly to the shunt controller, in this case though adjusting the series angle. The variables with a superscript *ref* can be specified and will become the reference values for the controllers' adjustment. The errors between the measured and
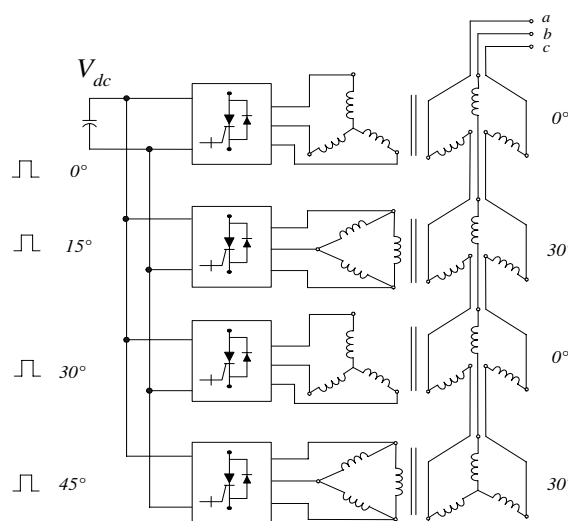


Figure 5: Generic arrangement for the HN technique
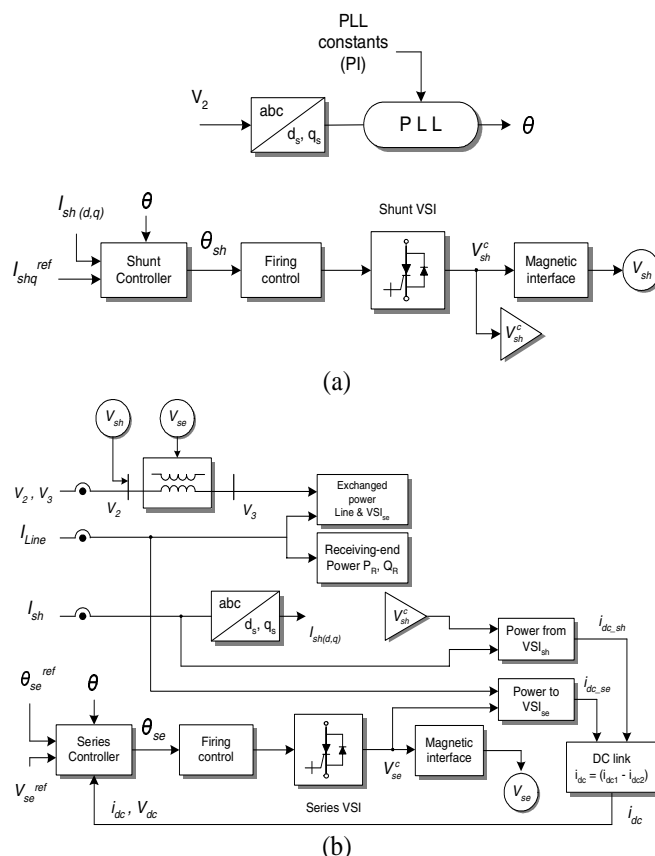


(a)



(b)

Figure 6: Simplified control block diagram of the UPFC

the specified values in each VSC are processed in a PI controller that computes the respective output variables.

On the other hand, the main parameters considered in the

Table 1: UPFC parameters

| Parameter | Value |
|---|---|
| Line nominal voltage | 138 kV |
| Apparent power | ±50MVA |
| Switching devices | GTOs – 24 pulses |
| DC link voltage | 25 kV |
| Coupling transformer X | 8% |

implementation of the UPFC, were (table 1):

The results corresponding to the steady-state operation of the UPFC, are shown in Fig. 7. Notice the output waveform of the shunt inverter ($V_{sh}$) depicted in Fig. 7(a) and the effect of the series voltage ($V_{se}$) over the power flow (Fig. 7b). The steady-state operation of the SSSC implemented, also showed satisfactory results. The SSSC implementation and waveform generation in ATP virtually followed the same procedure as its akin UPFC, except for the aforementioned quadrature operation of its series voltage imposed.

## 4 SIMULATION RESULTS

In this section, it will be shown the simulation results obtained in the ATP program. The system depicted in Figure 1, was used to simulate and assess the SSSC and the UPFC effectiveness in limiting the fault currents. For all the simulated cases (except Figure 10), the ground switch was set to produce the fault at t=0.1 s. Unless otherwise indicated, the results shown in this section pertain only to the contribution of the left-side AC system, with the measuring switch connected between the series coupling transformer and bus 3. The instant at which the series voltage is inserted was arbitrarily chosen. According to the tests carried out, it can with no restrictions be inserted at the very beginning of the fault.

### 4.1 SSSC case

Observe in Figure 8, the limiting effect of the series voltage ($V_q$=0.3 pu, inductive) when inserted to the line at t=0.20 s. Should a capacitive mode of compensation of the voltage $V_{se}$ be injected prior to the fault, the line fault current would increase as the relation $V_q/I_L$ will be seen by the system as a capacitive reactance which reduces the equivalent impedance of the line. This deleterious effect of capacitive compensation during faults, should also be taken into consideration.

On the other hand, a study regarding possible harmful effects of the short-circuit current upon the converters is also recommended to be performed, since the sudden increase of the line's current could be hazardous for the series inverter, specially if maintained for prolonged periods. Recall that the fault withstanding capability of the series VSCs depends
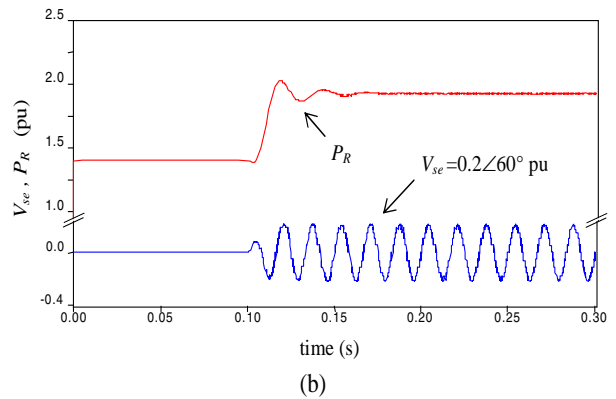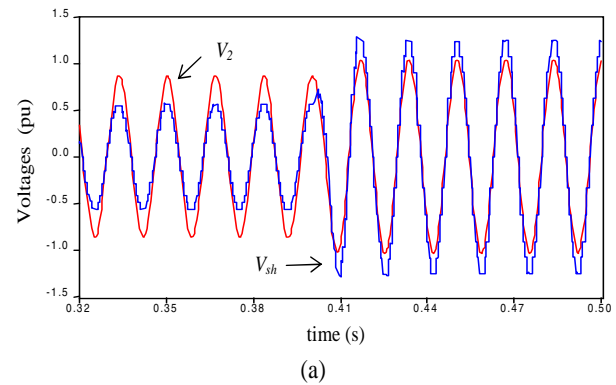


(a)



(b)

Figure 7: Equivalent (a) shunt and (b) series waveforms generated by the UPFC (quasi 24-pulse scheme)
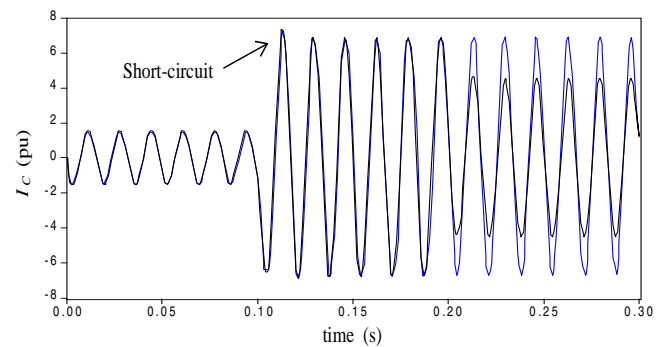


Figure 8: Limitation of the left-side current contribution by means of an SSSC. Tripolar short-circuit (phase C)

mainly on the characteristics of the power semiconductors within the inverters (Moran, 1996).

### 4.2 UPFC case

If during the fault period the series angle is set to operate with a value within the range $\theta_{se}$=120°→180°, a large series inductive reactance will be emulated, hence, a significant reduction of the short-circuit current, will be achieved.

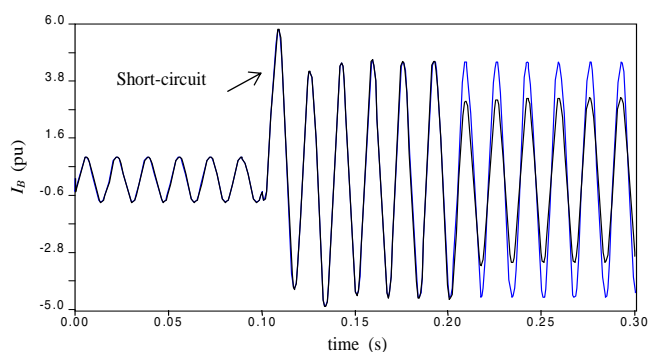Figure 9: Limitation of the left-side current contribution by means of a UPFC. Tripolar short-circuit (phase B)



Figure 10: Contribution of the shunt converter (VSC-1) to limit the left-side fault current (three-phase short-circuit)

The pre-fault angle of bus 3 is 15 degrees, which means that the referred voltage, thus the total fault current, can be minimized through an angle $\theta_{se}=165°$; whereas to minimize the left equivalent contribution, an angle equal to $\theta_{se}=180°$ in opposition to the 0° (degrees) of the left equivalent voltage, would be needed. The UPFC response towards the tripolar short-circuit current, is shown in Figure 9. The three-phase fault currents shown in Figures 8 and 9 were reduced in approximately 30%.

## 4.3 Shunt Converter Contribution to the Fault Current Limitation

As for the UPFC case, an additional strategy can be used to limit the fault current. Such a strategy consists in utilizing the shunt converter (VSC-1) so as to force the voltage, at the point where this converter is connected (therefore at the fault point), to reduce its magnitude. The total reduction of the short-circuit current in the left-side of the circuit goes from 16.66 pu (fault current amplitude in the time interval t=0.20→0.30 s) down to approximately 10.82 pu (Figure 10). This represents a reduction of about 44.58% in relation to the peak-to-peak current value existing during the no fault condition. The first limiting stage (t=0.30→0.40 s) pertains to the series voltage action (VSC-2), whereas the second one (t=0.40→0.50 s) to the effect of the shunt converter (VSC-1). This reduction strategy does not necessarily have to follow the sequence shown in Figure 10. In fact, both compensators should act simultaneously for a more effective fault current reduction.

The elapsed time with fault (t=0.20→0.30 s.) prior to the application of the series voltage, has also been chosen arbitrarily. It by no means indicates that this will be the time needed by the FACTS devices to respond or become effective. Actually, in order to avoid problems with the conventional protection system, this strategy should be applied at the onset of the fault. In this way, the current limitation ef-
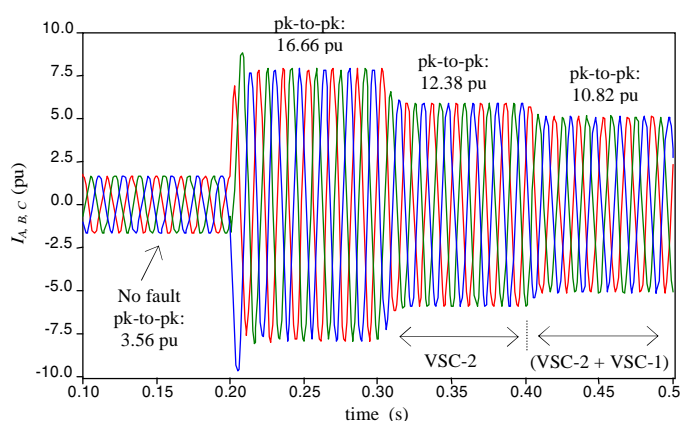
fectiveness will only depend on the stress that the semiconductor switches can withstand. Also, this current limitation strategy may imply both an appropriate rating of the converters and the strengthening of the series coupling transformer's iron, so as to avoid saturation.

## 4.4 UPFC Phase-to-Ground Fault

The results corresponding to the phase-to-ground fault analysis developed in Section 2, regarding the equivalent positive and zero sequence impedances of the left and right AC systems, are illustrated in Figure 11.

The total fault currents are reduced from 27.20 pu (uncompensated) down to about 23.05 pu and 19.25 pu, when the positive and the zero sequence voltages ($V_{se1}$ and $V_{se0}$) are applied, respectively. For this specific system, the series angles used were $\theta_{sea}=165°$, $\theta_{seb}=45°$, $\theta_{sec}=285°$ (for the positive sequence application) and $\theta_{sea}=\theta_{seb}=\theta_{sec}=165°$ (for the zero sequence application).

## 4.5 Further Comments

The three-phase faults simulated in the ATP program were applied to a balanced system. Likewise, the converter topology corresponded to a common neutral-point clamped three-level VSC converter. That is, no special type of converter was built. For practical applications, it would be advantageous to implement 2-level VSC-based converters. Although, as reported by Schauder *et alii* (1998) a 3-level inverter configuration (as the one utilized in the AEP Inez Station) could also be feasible and advantageous for real world applications. The use of 3-level inverter configuration is also becoming more common for assessing the FACTS devices' response in the research stage (Dufour and Bélanger, 2005; Ooi *et alii*,
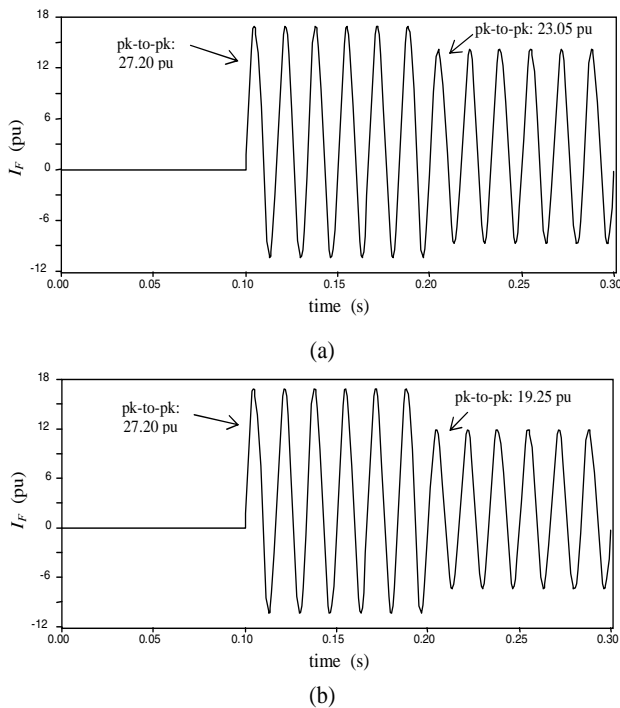
(a)



(b)

Figure 11: Total phase-to-ground fault current reduction: (a) Positive sequence application of $V_{se}$, (b) Zero sequence application of $V_{se}$

1999).

Of course, for phase-to-ground and bipolar faults the negative and zero sequence components must be incorporated in the ATP program. For both unbalanced systems and faults, it will be essential to have capability to inject different voltage phasors into all three phases, this research is currently underway.

Both shunt and series inverters have PI (Proportional-Integral) type of controllers that compare the reference (specified) parameters with those existing previously in the system. Also, the PLL (Phase-Locked Loop) controller used has no particular features. However, the idea while adjusting it was to find some PLL constants robust enough to operate under both normal and fault conditions, rather than building extra control systems aimed only to fault current limitation. For a proper operation of the converter (case of unbalanced systems) the PLL should be able to track adequately each phase (Song *et alii*, 1999; Kaura *et alii*, 1999).

The primary objectives of the FACTS devices regarded herein are the power flow control and the line voltage support. The short-circuit limitation strategy explored, showed that the SSSC and the UPFC may offer a useful additional functionality when implemented within the network.

## 5 CONCLUSIONS

This paper covered the main aspects of the steady-state AC series voltages when inserted into the power system during fault conditions. It has been observed that, aside of the power flow control characteristic and line voltage support, the series connected VSC-based devices considered (SSSC and UPFC) could be effective tools for limiting fault currents rather than being by-passed during such periods. Both devices may well overcome the continuously increasing short-circuit currents, resulting from the system expansion, which may jeopardize the fault current withstanding capability of existing assets.

The paper presented the basis to manipulate the series voltage in order to get the maximum effect while limiting short-circuits. Although in the analysis it was focused mainly the three-phase and line-to-ground faults for total and partial (branch contribution) fault currents, it could easily be extended to other type of faults. It has been shown that the UPFC shunt converter can also contribute to the reduction of the fault current. This can be achieved by forcing the line voltage to reduce its magnitude, thus, the fault current will do so. The magnitude of the series voltage used along the work was limited to 0.3 pu. The possibility to use higher values during short periods, could be translated in a more efficient compensation effect upon the short-circuit current. This aspect is still being investigated.

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