NORMALIZED STATICAL ANALYSIS WITH FREQUENCY AND LOAD VARIATION FOR THE CLASS-E CONVERTER BASED ON PIEZOELECTRIC TRANSFORMERS

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RESUMO

Análise Estática Normalizada com Variação de Frequência e Carga para o Conversor Classe-E utilizando Transformadores Piezoelétricos

Os transformadores Piezoelétricos permitem o projeto de aplicações promissoras para fontes de alimentação até 100W, melhorando a eficiência, reduzindo o tamanho, facilitando a obtenção de grandes relações de transformação, além de proporcionar alta imunidade contra ruídos eletromagnéticos e interferências. Por apresentarem um modelo elétrico equivalente de característica ressonante, utilizam-se topologias de conversores ressonantes para projetar estes conversores, como por exemplo, a topologia Classe-E. Para facilitar a análise de conversores de ordem superior, pode-se utilizar um método de análise normalizado. O controle do conversor Classe-E utilizando transformadores piezoelétricos é implementado através da variação da freqüência e da razão cíclica de operação. O ganho estático é regulado através da variação da freqüência de chaveamento, e a razão cíclica muda para atender as condições de comutação suave para diferentes freqüências. Este artigo apresenta uma análise completa normalizada deste processo, incluindo variação normalizada da frequência e carga, permitindo escolher um ponto ótimo de projeto estático e avaliar seu comportamento com a variação de frequência, sem a necessidade de parâmetros de projeto. São mostrados resultados experimentais para um conversor abaixador de 3W, para uma entrada universal de 85-260 V AC e saída de 6 V DC, para validar a metodologia apresentada.

PALAVRAS-CHAVE: Conversor Classe-E, Conversores Ressonantes, Transformadores Piezoelétricos, Análise Normalizada.

ABSTRACT

Piezoelectric transformers (PTs) allow the design of promising power supply applications, increasing efficiency, reducing size, facilitating the achievement of high transformation ratio, besides providing high immunity against electromagnetic noise. Due to the electrical equivalent model having resonant characteristics, some resonant topologies are used

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to build these power supplies, i.e. the Class-E converter. In order to make easier the analysis of high order converters, it's possible to use a normalized analysis method. The control of the Class-E converter using PTs is implemented through the switching frequency and duty cycle variation. The static gain is achieved though the switching frequency variation, while the duty cycle is adjusted with the purpose of achieving soft switching for different frequencies and loads. This paper shows a normalized analysis of this process, including a normalized frequency and load variation, without the need of design parameters. Experimental results for a 3W step-down converter are shown for a universal 85-260 V AC input and output voltage 6 V DC, to validate the proposed method.

KEYWORDS: Class-E Converter, Resonant Converters, Piezoelectric Transformers, Normalized Circuits Analysis.

1 INTRODUCTION

Piezoelectric Transformers (PTs) are an attractive option in order to reduce size, volume and weight in many low power applications (Yamane et al., 1998; Prieto et al., 2001). Building PTs into resonant topologies as Class-E, Half Bridge, Full Bridge, etc, provides high frequency and fast dynamical response designs (Yamane et al., 1998), allowing ZVS (zero voltage switching) without additional devices (Ninomiya et al., 1994). Therefore, PTs have been used in DC-DC converters (Yamane et al., 1998), CCFL (Cold-Cathode Fluorescente Lamps) backlighting inverters (Shoyama et al., 1997), offline power supplies (Diaz et al., 2001) and LED (light-emitting diode) lighting applications (Bisogno et al., 2006).

A normalized method was shown in (Kazimierczuk and Puczko, 1987), which allows the analysis of any converter using normalized graphics. The methodology avoids any parameter of the application, facilitating considerably the analysis and design of high order resonant topologies.

Later, (Bisogno et al., 2004; Yang et al.,2009) extended this idea, comparing the Class-E and Half Bridge piezoelectric converters. Static analyses concerning gain, ZVS conditions and the parameters selection have been presented. It was shown that this method favors the best operation point selection for each converter and allows a comparison between the topologies.

A dynamic model for the Class-E converter was presented by (Bisogno et al., 2005; Nittayarumphong et al., 2005). The method divides the converter in a low frequency circuit, related to the output filter, and a high frequency circuit, concerning the resonant part. The authors used frequency modulation (FM) in order to adjust the input-to-output gain to compensate input and load variations. However, the normalized methodology was not used. This inconvenience brings back the necessity of design parameters, as output power, input and output voltages, etc.

It is believed that analyzing high order power converter using the normalized method favors the optimum design and topologies comparison. So, an extended normalized overview which includes switching frequency and load normalized variations would be very useful. This paper has as the main contribution, the achievement of a static model of the converter, with normalized load and frequency variation.

2 NORMALIZED ANALYSIS OF THE CLASS-E CONVERTER

The purpose of the analysis is to obtain a numerical solution for many operation points so that is possible to compare them and obtain the optimum, without the parameters design. Independently of the operations point, it is forced that the converter operates under ZVS conditions.

Considering the Class-E topology builded with PTs as shown in Figure 1, the ZVS conditions are obtained when the voltage at the switch achieves zero naturally before it turns on.

Due to the low-pass filter characteristics of the PT, some simplifications can be done in the circuit according to (Bisogno et al., 2004). It is possible to assume the output rectifier plus filter as an equivalent resistance (R_{eq}), and after that controvert C_{d2} and R_{eq} to the primary side of the ideal transformer of the PT model. Therefore, the circuit becomes simplified as shown in Figure 2a.

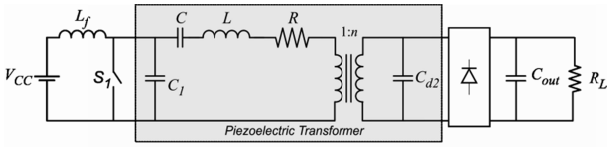
The components that are in parallel on the output can be considered as a series arrangement for a fixed switching frequency through Equation (1). Further, they can be rearranged with other elements in the circuit according to equation (2). The simplified circuit of Figure 2b is obtained.

$$R_{Seq} = \frac{{R_{eq}}'}{1 + {R_{eq}}'^2 {C_{eq}}'^2 \omega^2} \text{ and } C_{Seq} = \frac{1 + {R_{eq}}'^2 {C_{eq}}'^2 \omega^2}{{R_{eq}}'^2 {C_{eq}}' \omega^2} \quad (1)$$

$$R_S = R_{Seq} + RandC_S = \frac{CC_{Seq}}{C + C_{Seq}} \quad (2)$$

2.1 Normalization

The first step to normalize the system is based on the differential equations that describe the stages of the circuit. The stages are shown in Figure 3. The equations are obtained according to the circuit of Figure 2b as other authors already proposed (Bisogno et al., 2004; Yang et al., 2009). The waveforms of the circuit of Figure 2b are shown in Figure 4.



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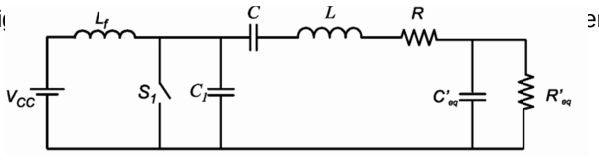

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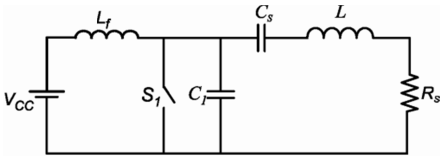
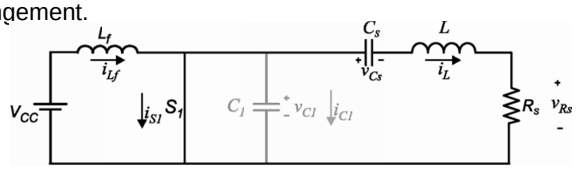


(b)

Figure 2: Simplified Class-E Converter. (a) Output elements in parallel arrangement. (b) Output elements in series arrangement.



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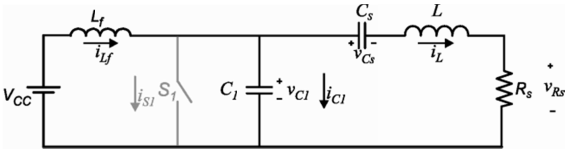


(b)

Figure 3: Stages of the converter at steady state. (a) Stage I - ($t_0 \leq t < t_1$: *DcT*). (b) Stage II - ($t_1 \leq t < t_2$: (1-Dc)T).

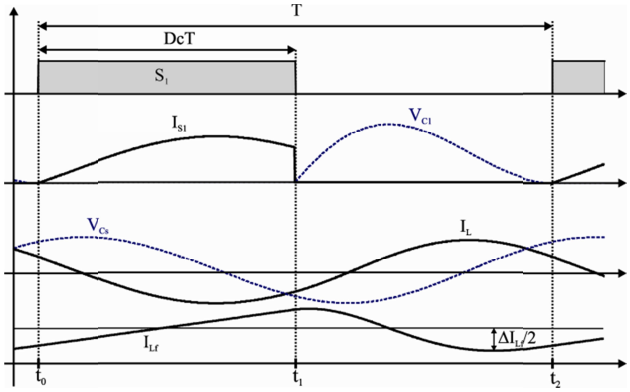


Figure 4: : Operation stages at steady state.

Where Dc is the Duty Cycle applied in the switch. The equations obtained have to be represented on state space form, as:

$$\dot{X} = AX + BU \tag{3}$$

As the system is described in two stages, two system will be created, $\dot{X}_{stage1}$and. The frequency and other parameters from the matrices can be eliminated through constants substitutions. These constants are defined regarding the relation between the resonances of the reactive component of the circuit and the switching frequency. Besides, quality factors are defined to eliminate the dissipative elements. These constants are defined as:

$$\begin{array}{c} \omega_1 = \frac{1}{\sqrt{LC_s}}, \omega_2 = \frac{1}{\sqrt{LC_1}}, \omega_3 = \frac{1}{\sqrt{L_f C_1}}, \\ A_1 = \frac{\omega_1}{\omega}, A_2 = \frac{\omega_2}{\omega}, A_3 = \frac{\omega_3}{\omega} \text{and} Q_1 = \frac{L\omega_1}{R_s} \end{array} \tag{4}$$

Where ω is the switching frequency. Thereby, the following normalized state space system can be achieved:

$$\dot{\begin{bmatrix} V_{c1}/V_{cc} \\ I_{S1}/I_{cc} \\ I_L/I_{cc} \\ \vdots \end{bmatrix}} = A_{(A_1,A_2,A_3,Q_1)} \cdot \begin{bmatrix} V_{c1}/V_{cc} \\ I_{S1}/I_{cc} \\ I_L/I_{cc} \\ \vdots \end{bmatrix} + B_{(A_1,A_2,A_3,Q_1)}.U(t) \tag{5}$$

The system is solved for many operation points using mathematic software. These points contemplate many different values of duty cycle, A_1, A_2, A_3, etc. Normally the input voltage basis is defined first (*Vcc*), but the input current basis depends on the equivalent DC resistance of the circuit (*Rcc*). The DC resistance can be defined as a constant (a) multiplied by the output equivalent resistance (*Rs*), as shown below:

$$R_{cc} = aR_s, \frac{V_{cc}}{I_{cc}} = aR_s \text{ and } \frac{P_o R_s}{{V_{cc}}^2} = \frac{1}{a} \tag{6}$$

The reverse of this constant, defined as $P_O R_S / {V_{CC}}^2$, is called power transfer ratio or quadratic static gain of the converter. The power transfer ratio is calculated according to:

$$\frac{1}{a} = \frac{{V_{O\_RMS}}^2}{{V_{CC}}^2} = \frac{{A_1}^2}{2\pi {Q_1}^2} \int_0^{2\pi} I_L(\omega_s t)^2 d\omega_s t \tag{7}$$

The details on how to obtain the normalized state space system and how to derive the power transfer ratio equations are shown in (Bisogno, 2006).

2.2 Normalized Static Analysis

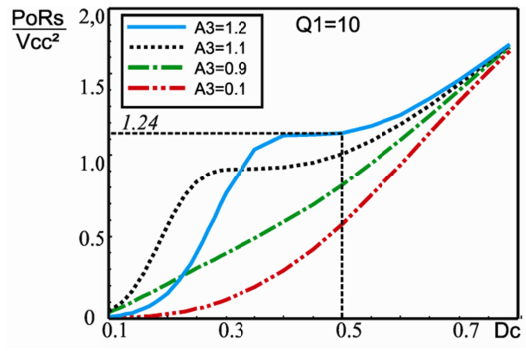
After obtaining the database with the numerical solutions for the Class-E converter for each operation point considering only the nominal frequency. It is possible to evaluate many normalized graphics, for instance, the gain variation for different duty cycles, as shown in Figure 5.

It can be seen in Figure 5a, that when Q_1 remains constant, the gain changes as a function of A_3. Dc=0.5 provides a

good gain in a flat region, with less sensitivity to the duty cycle derivation.

Assuming that A_3=1.2 and varying Q_1, the gain nearly doesn't change, as shown in Figure 5b. The variation of Q_1 means variation on the load of the converter. The output of the resonant circuit can be considered as a sinusoidal current source, and Q_1 variations can be neglected when Q_1>5.

There are other variables on the system that can be interesting for the design, for instance, normalized voltage (V_{S_pk}) and current (I_{S_pk}) peaks at the switch. The curves can be observed in Figure 6.



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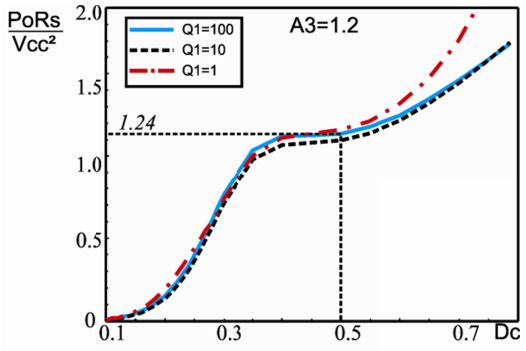
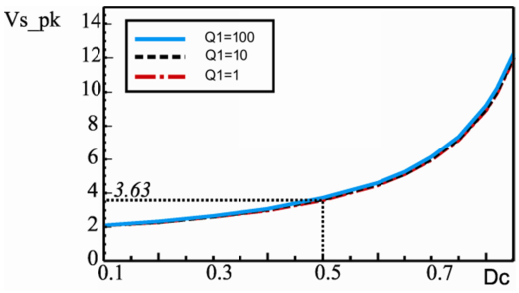


(b)

Figure 5: Power transfer ratio as function of the Dc, A_3 and Q_1. (a) A_3 Variation. (b) Q_1 Variation.



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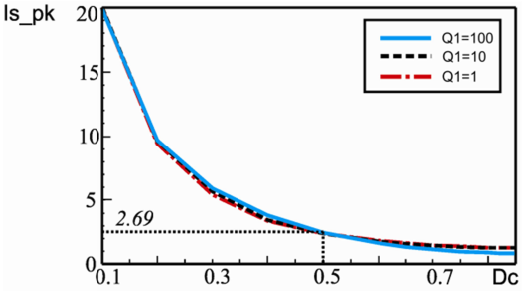

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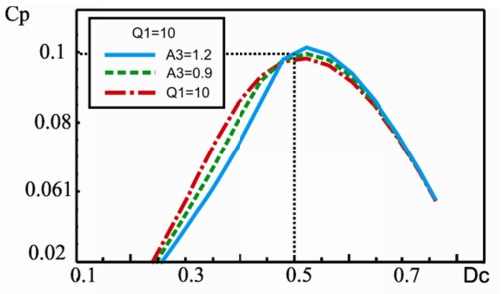


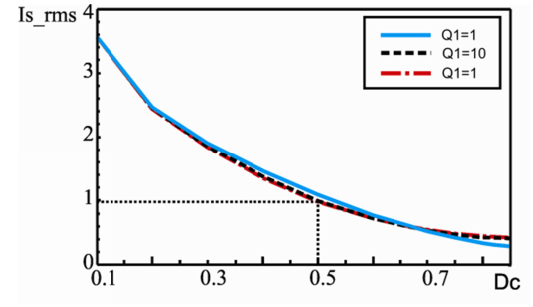
(c)

Figure 6: Normalized voltage and current peak in the switch as a function of the Dc and Q_1. (a) Voltage. (b) Current. (c) C_p, normalized distribution.

It can be implied from Figure 6 that designing the nominal point for low or high duty cycles, entails on high current or high voltage stresses respectively. It is possible to play with the design point from the right to the left depending on the switch technology and converter input voltage. In other words, it is possible to find a balance between voltage and current peaks. The point Dc=0.5 shows an equilibrium between the extremes. It can be confirmed by the curves in Figure 6c, obtained through the equation (8) for different values of A_3:

$$Cp = \frac{1}{V_{s\_pk} I_{s\_pk}} \tag{8}$$

The voltage and current peaks on the switches don't change significantly for Q_1 and A_3 variations. The normalized graphic of the rms current in the elements can imply the point where the converter becomes lossier. It is defined I_{S_rms} and I_{Lf_rms} as the rms normalized current in the switch and the input inductor respectively. Both are shown in Figure 7.



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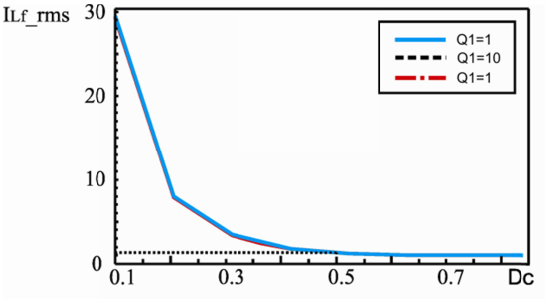


(b)

Figure 7: Rms current in the inductor and in the switch as a function of Dc and Q_1. (a) Current in the switch. (b) Current in the inductor.

It is possible to infer from Figure 7 that the losses are lower for higher duty cycles. Other elements from the circuit belong to the PT, so the losses are not considered. The efficiency of the PT is near the unity (up to 97%) and its losses are not directly proportional to the current, but to physical characteristics related to mechanical oscillation.

3 STATIC MODEL WITH FREQUENCY VARIATION

When the circuit has to be normalized only for nominal frequency analysis, the circuit from Figure 2b returns precise results (Bisogno et al., 2004). However, when the switching frequency changes, the simplification represented by the equation (1) prevents the results to be correct, due to ω in the equation. This means that the approximation is valid only for the nominal frequency. To correct that, the differential equations have to be obtained according to the circuit of Figure 2a, not the one from Figure 2b as other authors proposed (Bisogno et al., 2004; Yang et al.,2009). The state space equations are again obtained. The frequency and other parameters from the matrices are again eliminated through constants substitutions. Due to the circuit change, new constants are defined in :

$$\omega_4 = \frac{1}{\sqrt{LC'_{eq}}}, \omega_5 = \frac{1}{\sqrt{LC}}, A_4 = \frac{\omega_4}{\omega}, \\ A_5 = \frac{\omega_5}{\omega}, \text{and} Q_4 = \frac{L\omega_4}{R'_{eq}} \quad (9)$$

Where ω is the switching frequency. Thereby, the normalized state space system represented by can be achieved:

$$\begin{bmatrix} \dot{V}_{c1}/V_{cc} \\ I_{S1}/I_{cc} \\ I_L/I_{cc} \\ \vdots \end{bmatrix} = A_{(A_1,A_2,A_3,A_4,A_5,Q_1,Q_4)} \cdot \begin{bmatrix} V_{c1}/V_{cc} \\ I_{S1}/I_{cc} \\ I_L/I_{cc} \\ \vdots \end{bmatrix} \\ + B_{(A_1,A_2,A_3,A_4,A_5,Q_1,Q_4)}.U(t) \quad (10)$$

After the selection of the nominal operation point according to curves as shown in section 2, it is possible to verify how the output can be regulated. As show in (Yang et al., 2004) for different resonant converters topologies, the regulation is achieved through the switching frequency variation close to the resonance of the resonant tank. The maximum gain is achieved at the peak of the resonance. (Yang et al., 2004) also infers that is possible to have ZVS when the converter works on the right side of the resonance curve. The input-to-output regulation can be achieve through the frequency adjust concerning curves as in Figure 8. These are hypothetical gain curves for the circuit in Figure 1a, considering different loads represented by Q_1.The nominal operation point is given for minimum Q_1, where the maximum power transfer is achieved. The load at this point respects the equation (11):

$$R'_{eq} = \frac{1}{\omega C'_{eq}} \quad (11)$$

Assuming that Q_1 minimum is equal 1 as shown in Figure 8, the maximum gain is obtained at the peak of the admittance curve (f_{O1}). However, (Diaz et al., 2004) showed that when ZVS is required, it is necessary to have a distance between the resonance peak and the minimum operation frequency. The reason is that some reactive energy is necessary to achieve ZVS. At the peak, current and voltage are totally in phase to each other. Besides, the sensitivity at this point is too high.

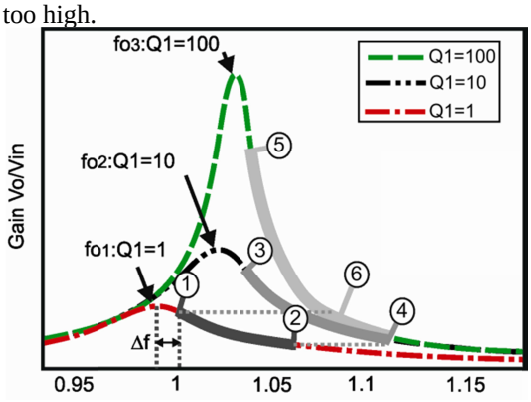


Figure 8: Operation regions and resonance frequencies.

This difference is defined as Δf, and implies that the minimum switching frequency has to be f_{O1}+Δf for nominal load. For other loads, the minimum frequency changes due to

the resonance frequency variation, f_{O2} and f_{O3}. Therefore, it is assumed that the minimum switching frequency is placed at the point 1 in Figure 8. This point has the maximum gain keeping ZVS, and the frequency can be increased to regulate the converter, for instance the point 2.

When the load changes to Q_1=10 or Q_1=100, the ZVS regions become 3-4 e 5-4 respectively. Nevertheless, the maximum gain is defined by the nominal load at point 1, limiting the operation between 6-4 for Q_1=100, not 5-4 anymore.This statement induces to the conclusion that the minimum switching frequency takes place at point 1. This is an important conclusion in order to justify the control strategy shown in Figure 9. It is based on the switching frequency and duty cycle variation, always for frequency values higher than the nominal one, at point 1.

To work in this way, the output voltage has to be measured and compared to the reference value. The error is compensated and the control voltage goes to a VCO (Voltage Controlled Oscillator). The VCO provides the triangular wave which has the switching frequency information.

It is important to observe that the normalized analysis method shown in the sections 1 and 2 find always the solution for the point 1 in Figure 8. Thus, the frequency variation is not considered. However, if the switching frequency increases as a result of the control strategy, the switch turns on while the current goes through the anti-parallel diode, as shown in Figure 10b.

The current (I_{S1}) and the voltage (V_{S1}) in the switch for a nominal operation point ($f_S/(f_{O1}+\Delta f)$=1) are shown in Figure 10a . This point is the point 1 in Figure 8. Figure 10b shows the behavior after the frequency being increased. There is a duty cycle window which is shown in Figure 10b. It is defined by the time while the current crosses the anti-parallel diode of the switch. These windows change for each frequency value, but for any point inside this window ZVS can be achieved.

Figure 11 helps to understand the modulator behavior in the control loop from Figure 9. It is suppose to generate a triangular wave with variable frequency according to the VCO input voltage, and a duty cycle that respects the ZVS conditions. To respect the ZVS conditions, it is necessary to implement a function that adjusts the duty cycle. This function is called duty cycle tracking. So, the main contribution of this paper is the analysis the frequency, load and input variation using the normalized concept, in order to obtain the general duty cycle window of the class-E converter.

So, the main contribution of this paper is the analysis of the frequency, load and input variation using the normalized concept, in order to obtain the general duty cycle window of the class-E converter. With this achievement, it possible to understand the behavior of the circuit for all conditions, and implement the duty cycle traking in the modulator. Figure 12 shows the so called duty cycle window for different Q_1 and A_3. It can be seen that for different loads, with A_3 constant, the duty cycle window changes considerably in Figure 12a.

For Q_1 constant, depending on A_3, there are different regions for the duty cycle in Figure 12b. It can be seen that A_3=1.2 provides bigger ZVS region.

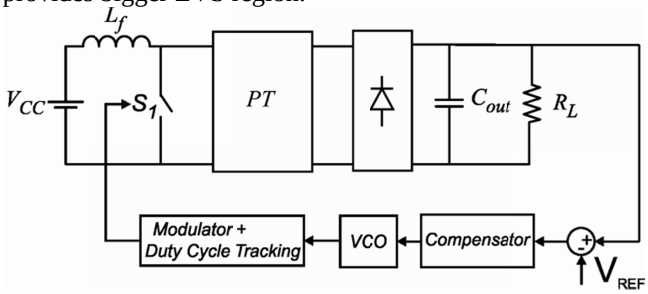


Figure 9: Control System for the Class-E Converter.

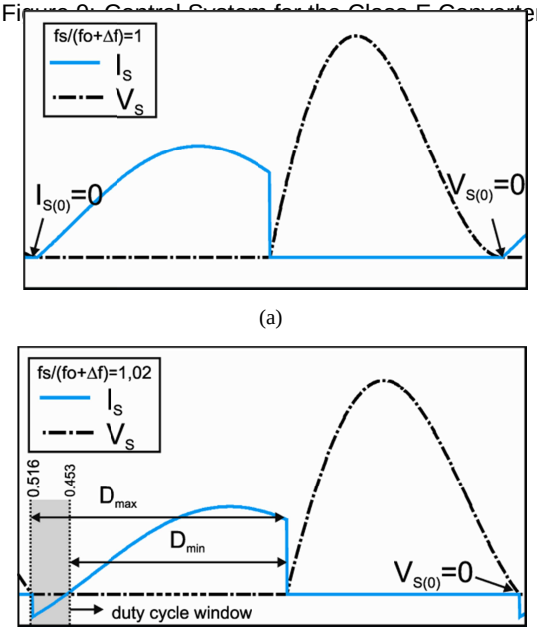


Figure 10: Current and voltage in the switch for different switching frequencies. (a) Nominal frequency. (b) Higher frequencies.

The operation point of Figure 12b, is also represented in Figure 10b, for A_3=0.1 e $fs/(fo+\Delta f) = 1.02$. Figure 13 shows the normalized static gain considering load and A_3 variations. The relation among the gains is defined as:

$$\frac{P_o R_s}{{V_{cc}}^2} = \frac{Icc^2}{Io^2} = \frac{Vo^2}{Vcc^2} \tag{12}$$

It can be inferred from Figure 13, that higher A_3 provides higher gain at all frequency range. On the other hand, the

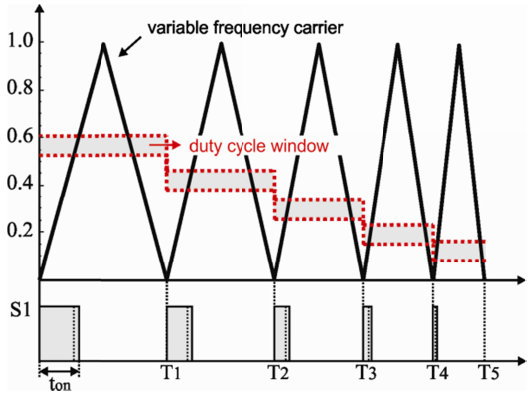
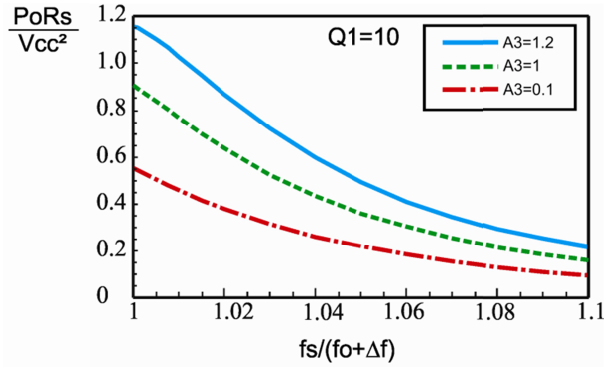


Figure 11: Modulator functionality.

higher the quality factor, the lower the frequency range necessary to change from the maximum to the minimum gain.



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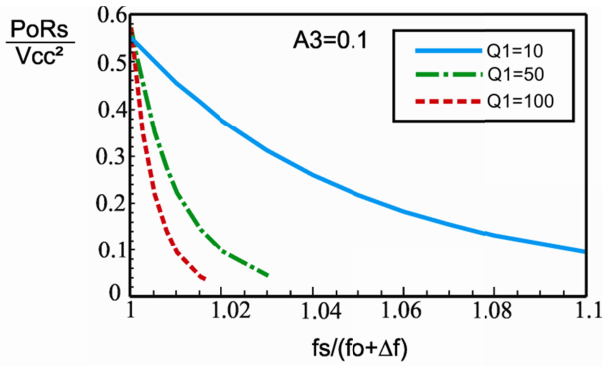


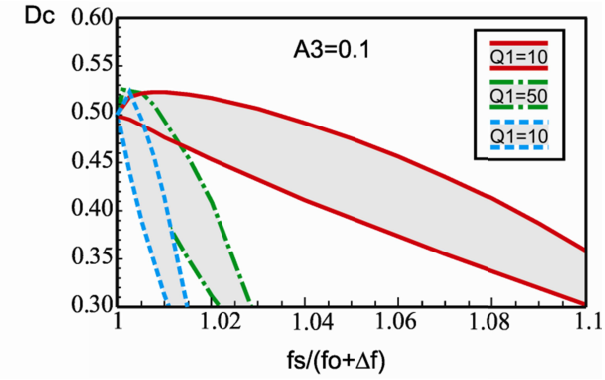
(b)

Figure 13: Normalized gain vs. switching frequency. (a) Constant Q_1. (b) Constant A_3.

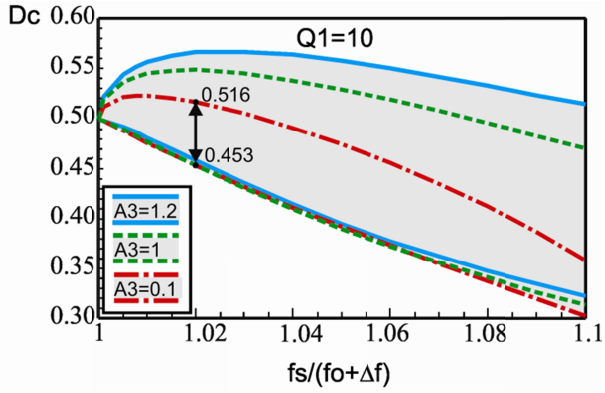
4 NORMALIZED REGULATION WITH FREQUENCY AND LOAD VARIATION

In order to know the behavior of the circuit for the whole operation range, the load variation has to be included in the analysis. To explain how it works, four boudary operation points were defined, as shown in Figure 14.

Figure 14a shows the frequency response of the converter regarding the gain for different loads. Figure 14b shows a



(a)



(b)

Figure 12: Duty Cycle window vs. frequency. (a) Constant A_3. (b) Constant Q_1.

zoom of the operation region. The four corners of the operation region are defined as:

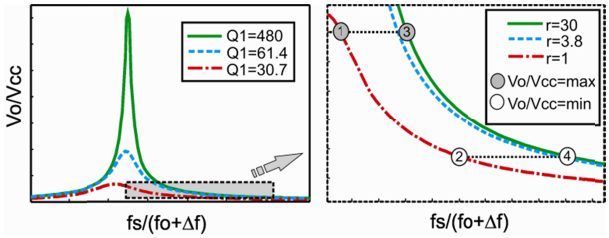
Point 1 – Lowest input voltage, lowest switching frequency, nominal load and highest gain. This is the design point obtained according to the method shown in section 2.

Point 3 – Lower input voltage, higher gain, minimum load. The minimum load is defined as thirty times the nominal one. It is not necessary to sweep the load further, because the bahavior remains the same.

Point 2 – Higher input voltage, minimum gain, nominal load.

Point 4 – Higher input voltage, minimum gain, minimum load.

First, for the maximum gain, the load was changed from the nominal (point 1) to minimum load (point 3). The output was suppose to be constant. When the load changes from full to light load, the gain increases, so the frequency has to increase to compensate the gain. This process provides the first curves in the left of Figure 15, which are highlighted with the numbers 1 and 3 on the extremes. Some simulations were done



(a) (b)

Figure 14: Operation region. (a)Gain curves. (b) Zoom at operation region.

for gains in between the maximum and the minimum. These curves help to assure that the duty cycle window exists for the whole operation range.

Finally, for the minimum gain, the load was sweeped from nominal value (point 2) to light load (point 4). This process provides the last curve on the right of Figure 15, which is highlighted with the numbers 2 and 4 on the extremes. The upper part of the curves means the maximum duty cycle and the lower part, the minimum. As the simulations consider all possibilities of frequency, gains and loads, the result obtained is called global duty cycle window.

With this method is possible to analise the global duty cycle window for different nominal designs parameters as shown in Figure 16. Figure 16a shows the global duty cycle windows for three different designs regarding A_3. The same sweep proceedure from Figure 15 were done. It is clearly noticed that higher A_3 provides bigger duty cycle window. While for A_3=0.1 is not possible to achieve ZVS for the whole operation range. The limits where the solution does not exist are represented by the letter "X" at the Figure.

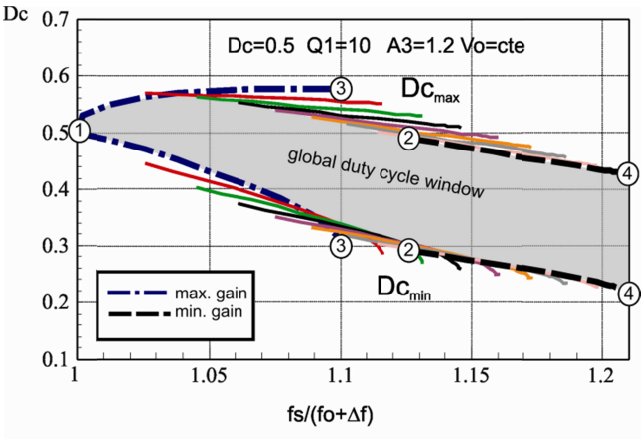
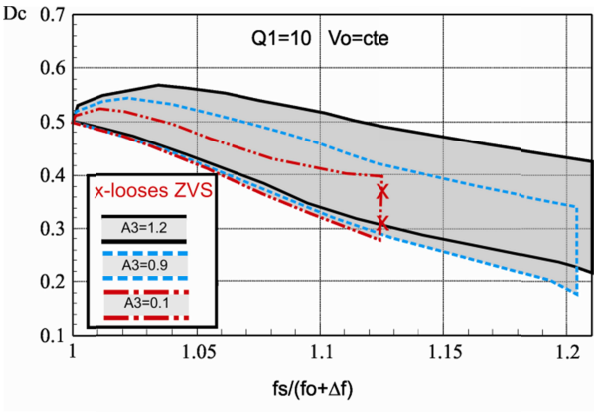
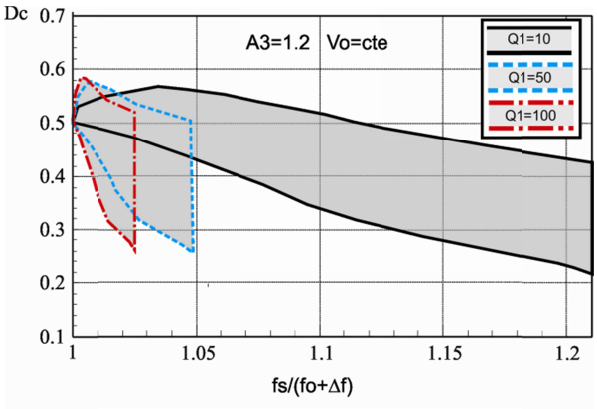


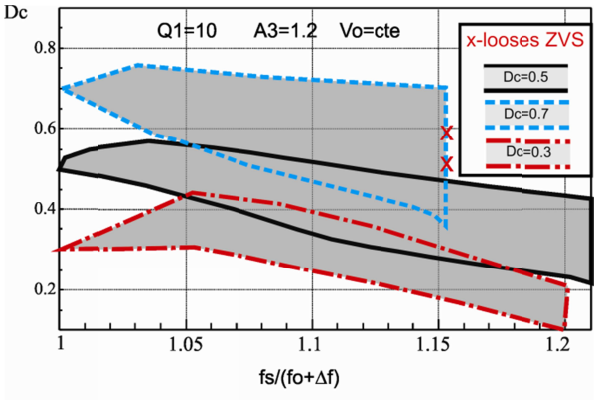
Figure 15: : Global duty cycle window.



(a)



(b)



(c)

Figure 16: Global duty cycle window (a) Different A_3. (b) Different Q_1. (c) Different Dc.

Figure 16b shows the window for different quality factors. The results are the same range of duty cycle, but in a small range of frequency. It means that for higher Q_1, a lower frequency variations has to be applied to reduce the gain. This was expected once the curves become sharper.

Figure 16c show different duty cycle designs. The result shows that for Dc=0.7 is not possible to find solution for all frequency and loads for the circuit normalized parameters.

On the other hand, for higher duty cycles the windows become bigger.

Finally is possible to design the system through two curves only, as shown in Figure 17. The operation points, 1, 2, 3 and 4 are detailed in the Table 1. Using the minimum and maximum frequency values is possible to build a function for the desired duty cycle.

Table 1: Operation points from Figure 17.

	Point 1	Point 2	Point3	Point 4
Vo/Vcc	1	1/3	1	1/3
fs/(fo+Δf)	1	1.041	1.032	1.073
r	1	1	30	30
Dc	0.4	0.22-0.36	0.24-0.47	0.18-0.3

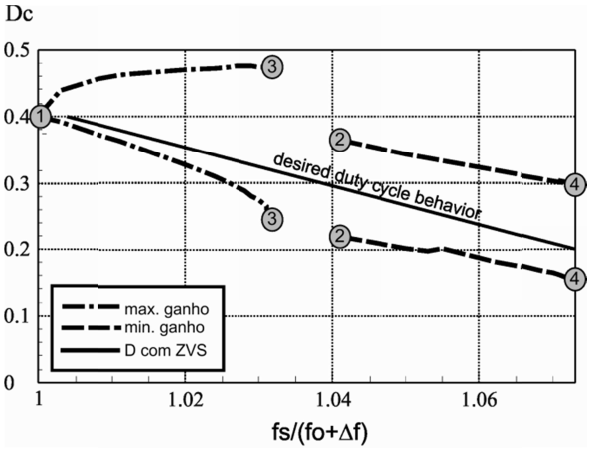


Figure 17: Desired duty cycle behavior.

5 EXPERIMENTAL RESULTS

A 3W Classe-E piezoconverter was implemented to validate the theoretical results. The PT used is the same device as (Bisogno et al., 2004). The parameters are shown in the Table 2 and a picture of the transformer in Figure 18.

The PT behavior was tested through frequency response measurements using the equipment [AP200]. The measurements where done for different loads shown in Table 2, as shown in Figure 19a. The highlighted region is zoomed in Figure 19b.

Figure 20 shows the experimental curves obtained with nominal load (Q_1=30.7) for the same frequencies highlighted in Figure 19b, fs=157kHz and 166kHz. For these two points, the used duty cycles, and the allowed ones (Dc window) are shown in the Table 3. This table also shows the rms voltage in the output resistor (R_{eq}). It is important to observe that for this design, although the resonance frequency is around 155 kHz, the first point to provide ZVS is 157 kHz. This value is given by A_1 and represent the point $f_S/(f_{O1}+\Delta f)=1$.

Figure 21 shows the comparison between the experimental and the theoretical results for the duty cycle window and the normalized gain. It can be inferred from the results that the developed analysis is valid and provides good results.

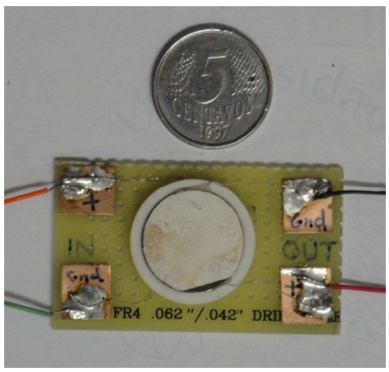
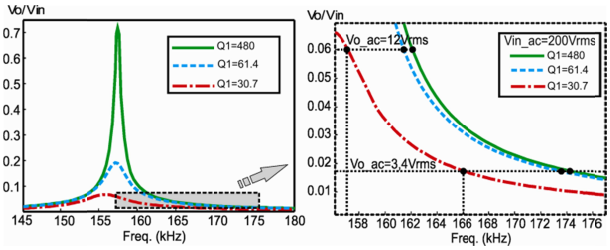
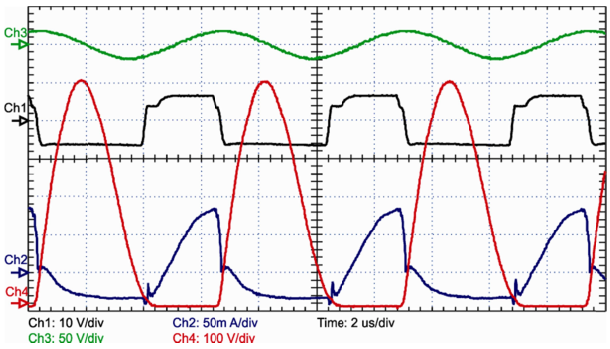


Figure 18: Piezoelectric transformer used for the implementation.

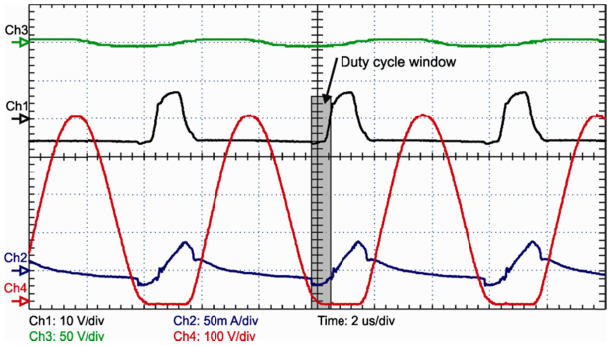


(a) (b)

Figure 19: Frequency Response of the PT. (a) Gain Vo/Vin. (b) Zoom.



(a)



(b)

Figure 20: Experimental results, Ch1=Gate of the switch, Ch2=Voltage at the output resistor (R_{eq}), Ch3= Current in the switch plus parasitic capacitor and Ch4=Switch voltage. (a) fs=157kHz. (b) fs=166kHz.

Table 2: Parameter of the Implemented Converter.

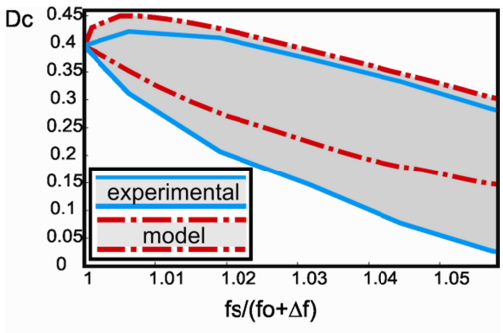
Parameter	Value	Unit
Vin_ac	85-260	V
fs	155...172	kHz
Vo_rms	6	V
Po	3	W
Q_1	30.7-61.4-480	-
R_L	12-44-360	Ω

Table 3: Experimental results for Vcc=200V.

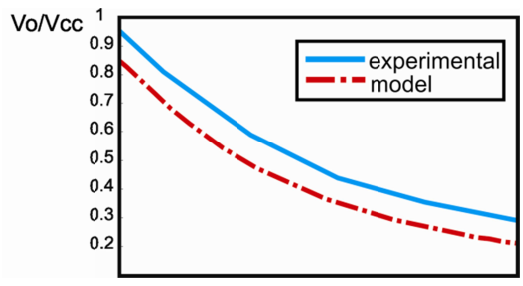
fs	Applied Dc	Dc window	Vo_rms
157kHz	0.4	0.4	12.5
166kHz	0.15	0.05-0.28	3.7

In Figure 21a, it's seen that the real duty cycle window is even bigger then the theoretical one. In Figure 21b can be seen that the the curves are close and parallel to each other. There is a small DC error that can be easily eliminated by the integral part of the compensator when the closed loop be implemented.

Figure 22 shows the comparison among the model, the SPICE simulation and the experimetal results for the global duty cycle window. Four different loads were selected for the measuremets. Figure 22a shows the results for the maximum gain at Vcc=120V, while the Figure 22b ilustrates the results for an intermediate gain at Vcc=180V. It can be seen a small deviation on the experimental curves. However, there is always a common region between model and measurements. The results induce to the conclusion that the duty cycle function should be implemented near to the lower curve given by the model. This would guarantee ZVS for all operation range.

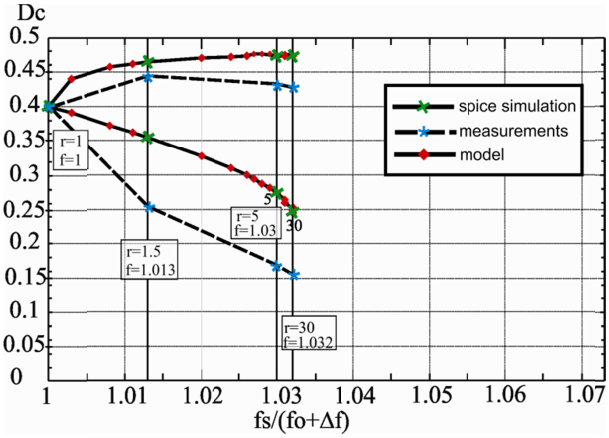


(a)

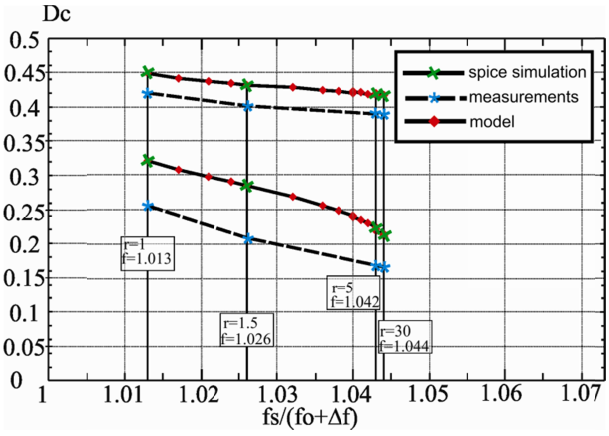


(b)

Figure 21: Results comparison between theory and experiments. (a) Duty cycle window. (b) Gain Vo/Vin.



(a)



(b)

Figure 22: Experimental results of the global duty cycle window. (a) For minimum input voltage, Vcc=120V. (b) For 1.5 times the minimum voltage, Vcc=180V.

It is important to point out that the small deviation between the theory and experimental results are given by neglected parasitic components. One of the simplifications is the efficiency of the transformer, which is considered as unity. A parasitic element that influences a lot the circuit is the switch capacitance. The probes capacitance interfere as well, and can be considered in future works.

6 CONCLUSIONS

This paper shows an extension on how to analyze resonant converters based on a normalized methodology. The theory was applied to the Class-E topology with piezoelectric transformers, due to the promising characteristics of this combination, as reduced size, weight, etc.

Former papers introduced the normalized method to design the nominal point of the converters, regardingless the overall operation range.

The whole operation range was considered in this work. The switching frequency and the load where sweeped to obtain the global duty cycle window of the circuit. This window defines which duty cycles should be applied for each switching frequency in order to obtain ZVS. This information is used to implement the modulator and is called duty cycle tracking .

These results allow to achieve the optimum desing point which considers the complete operation of the converter, including frequencies and loads.

The methodology was validated experimentally with a 3W step-down prototype. It was designed for universal input, 85-260 V AC, and an output of 6 V DC.

The SPICE simulation and the mathematical model are completely in agreement. The model and experimental results are in agreement with a small deviation given by neglected parasitic components. The results help to understand the complex behavior of such a converter.

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