A THREE-PHASE TO THREE-PHASE MATRIX CONVERTER PROTOTYPE

Milton E. de Oliveira Filho*
milton.evangelista@ufsc.br

Alfeu J. Sguarezi Filho†
alfeu.sguarezi@ufabc.edu.br

Ernesto Ruppert‡
ruppert@fee.unicamp.br

*Mobility Engineering Center, Federal University of Santa Catarina - UFSC, Joinville-SC

†Center of Engineering, Modeling, and Applied Social Sciences - CECS,
Federal University of ABC - UFABC, Santo André-SP

‡Department of Systems and Energy Control, Electrical and Computer Engineering,
University of Campinas, Campinas-SP

RESUMO

Protótipo do conversor em matriz trifásico para trifásico
Este trabalho apresenta aspectos relacionados a implementação experimental de um conversor trifásico em matriz. As chaves bidirecionais empregadas na construção do protótipo foram construídas com a utilização de componentes discretos como IGBT's e diodos rápidos. Aspectos relacionados a proteção contra sobre tensão e curto circuito, processo de comutação das chaves bidirecionais e filtro de entrada são apresentados neste trabalho juntamente com resultados experimentais da operação do conversor.

PALAVRAS-CHAVE: Conversor em matriz, Chave bidirecional, Modulação por vetores espaciais, Filtro de entrada, Varistores.

ABSTRACT

This paper presents some implementation details of a three-phase to three-phase matrix converter prototype. The bi-directional semiconductor switches were built using discrete IGBTs and fast diodes. Design aspects such as protection against overvoltage and short-circuit, commutation process of bi- directional switches, and input filter are addressed in this paper.

KEYWORDS: Matrix converter, Bi-directional switch, Input filter, Safe commutation, Space vector, Varistors.

1 INTRODUCTION

The three-phase voltage source inverter is widely used as power converter in many kind of applications and exist in literature several studies (Michels et al., 2005; Gabe et al., 2009). Although this kind of converter has a mature technology and robustness, the presence of a large electrolytic capacitor in the dc link causes a high-distorted input current with THD that can be over 140% as well as increases the costs. The matrix converter is a forced commutated converter which can perform the power conversion directly from AC power source to the load without any intermediate DC link. The matrix converter scheme, shown in Fig. 1, consists of an array of bi-directional power switches arranged in a matrix manner so that any output of the converter can be connected directly to any input voltage source. The idea of the matrix converter was first presented in Gyugyi and Pelly (1976) but the increasing interest on matrix converter began with Venturini (1980) where it was presented a method to control the matrix converter operation known as Venturini modulation method.

Artigo submetido em 23/04/2010 (Id.: 1132)
Revisado em 18/09/2010, 15/07/2011, 30/08/2011
Aceito sob recomendação do Editor Associado Prof. Takashi Yoneyama

In addition to the lack of the expensive DC link, which makes the matrix converter a compact power electronics circuit, other desirable features like sinusoidal input currents, regeneration capability and high power factor operation are considered for high performance application.

Despite of all mentioned advantages, the matrix converter doesn't have a spread use as power converter in the industry. Matrix converter suffer from important drawbacks as: the voltage ratio is lower than unity, the unbalance and distortions at the input voltages are immediately reflected to the load side and complex protection issues. Besides this, since there isn't an useful bi-directional switch semiconductor device in the world market, it is necessary the use of 18 unidirectional semiconductor devices, like MOSFETs and IGBTs, to construct a three-phase matrix converter increasing the overall costs.

Although those drawbacks limit the applications of the matrix converter there are many publications reporting the use of the matrix converter to feed induction motor drives (Khwan-on et al., 2010; Lee and Blaabjerg, 2005; Cha and Enjeti, 2004; Wang et al., 2010). Although many papers show experimental results, fewer paper deals specifically with the design of matrix converter (Xie and Ren, 2004; Sokolovs and Galkin, 2008; Klumpner et al., 2002; Wheeler et al., 2004; Saengseethong and Sangwongwanich, 2010; Mohite and Gujarathi, 2010). Usually these papers cover some design aspects of the matrix converter but other aspects are not treated deeply to give enough information of how to build a matrix converter in detail.

This paper deals with a low power matrix converter prototype design and implementation in the laboratory with the objective of driving a three-phase RL load. The pulse width modulation algorithm used in this paper is the space vector modulation, which allows the matrix converter operates with the maximum voltage gain for matrix converter using simple calculation. The idea of this work is to help designers in the matrix converter prototype implementation.

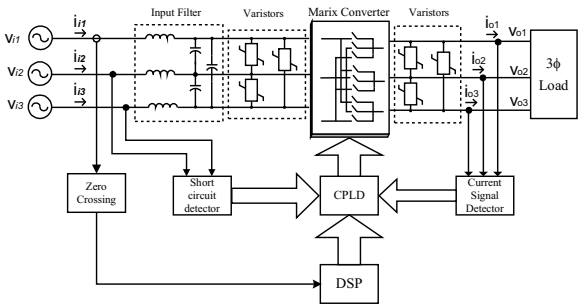


Figure 1: The Three phase to three-phase matrix converter.

2 THE MATRIX CONVERTER DESIGN

A schematic diagram of the matrix converter can be seen in Fig. 1. The design of the matrix converter treated here comprises both hardware and software implementation. In the hardware implementations it will be treated the bi-directional switches realization, the gate drive circuits, the safe commutation and protection of the bi-directional power switches, and the input filter design. The heatsinks of the power switches was designed in accordance with Pomilio (2006). The software implementation concern the implementation of the space vector modulation for matrix converter in the DSP TMS320F2812.

2.1 Bi-directional switches realization

2.1.1 Bi-directional switches

The matrix converter uses nine power bi-directional switches. A bi-directional switch, shown in Fig. 2(a) must be able to block direct and reverse voltage and to conduct the current in both directions. Bi-directional power switch is one of the major challenges for the power stage design of a three-phase to three-phase matrix converter since bi-directional power switches are not available in the market. Recently some power electronics devices manufacturers have tried to produce experimental bi-directional power switch modules for matrix converter. These power modules are implemented with unidirectional switches like as IGBTs and fast diodes (DIM200WBS12-A000, SML300MAT06 and FM35R12KE3). Furthermore, some research groups have been using a specially designed power modules to build the matrix converter (Klumpner et al., 2002; Adamek et al., 2003; Simon et al., 2002). Unfortunately, these power modules are not produced in industrial scale, so their cost is very high making difficult their use in a laboratory prototype since if part of the module fails, the entire unit must be replaced. So, it is cheaper to build the bi-directional power switch using discrete components.

Three possible ways to obtain a bi-directional power switch using low costs commercial IGBTs are shown in Fig. 2. Another possibility to get a bi-directional switch is the use of two reverse blocking IGBTs in anti-parallel connection (IXRA15N120) (Takei et al., 2003).

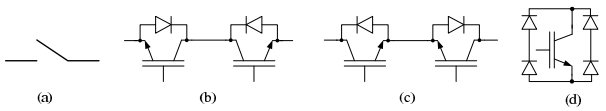


Figure 2: Bi-directional switches: (a) ideal switch (b) common collector switch, (c) common emitter switch and (d) diode bridge switch.

The topology based on diodes bridge, as shown in Fig. 2(d), causes higher conduction losses since the current path is formed by two diodes and one IGBT and this is the reason why it is less used than the other topologies. The gate drive circuitry is simple since there is one controlled component in each power bi-directional switch. On the other hand, the topologies based on common collector or common emitter connections of two IGBTs, as shown in Fig. 2(b) and (c) respectively, allow lower conduction losses and are commonly used in the matrix converter design, but the use of two IGBTs increases the complexity of the gate drive. It is necessary a total of eighteen IGBTs and eighteen diodes to build the three-phase to three-phase matrix converter using both common collector and common emitter topology. So, the choice of bi-directional switch implementation will influence the hardware requirements to build the matrix converter.

The design of the power stage of the matrix converter is facilitated if the nine bi-directional power switches are grouped in 3-to-1 phase power modules. Using IGBTs with co-pack fast diodes, like as the IGBT IRGB15B60KD, it is possible to reduce the number of discrete power components in the power modules.

in Fig. 3 it is shown a 3-to-1 phase power module using the common collector configuration. Using this topology it is necessary only six isolated power supply to feed all the gate drives in the three-phase matrix converter: while one isolated power supply can supply the gate drives of the IGBTs connected in the same output, for example Sa2, Sb2, and Sc2, an isolated power supply is necessary to feed the gate drives of the IGBTs connected in the same input phase. Since they are located in the two other power modules, there are connections between the power modules making more complicate to make tests in each power module separately. On the other hand, the common emitter configuration, as shown in Fig. 4, was chosen due to the possibility to construct a three-phase matrix converter using 3-to-1 phase power modules without external connection between the modules since one isolated power supply feeds the gate drives of the IGBts forming a bi-directional switch, as shown in Fig. 5. The drawback of this configuration is the need of nine isolated power supplies; three more than the common collector configuration, but this approach facilitates the tests of the power stage of the matrix converter.

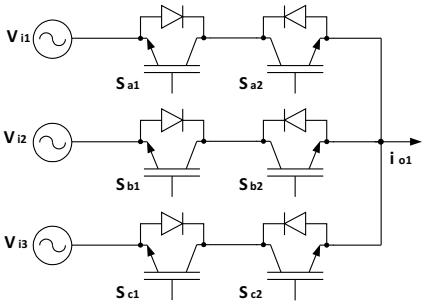


Figure 3: A three-phase to one-phase matrix converter module using common collector configuration.

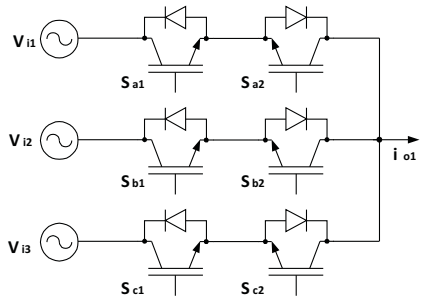


Figure 4: A three-phase to one-phase matrix converter module using common emitter configuration.

2.1.2 Gate drive circuitry

The gate drive circuitry transfers the information from the control circuit to the power bi-directional switches and must provide isolation between them. There are several approaches to perform the gate drive isolation: pulse transformer, with optocoupler, bootstrap circuit and photovoltaic cell. Pulse transformer and photovoltaic cell approaches simplify the gate drive circuit since it is not necessary the use of isolated power supply. The drawback of the pulse transformer approach is that it does not work very well for a PWM signal with wide duty cycle: the duty cycle is limited to 50%. For operation with duty cycle from 1% to 99%, it will be necessary some external circuitry to implement a DC restorer and an interface circuit with the CPLD. Other drawback is the large volume occupied in the PCB (Printed Circuit Board). The photovoltaic cell has low efficiency to transfer energy to the gate drive and the power level is not enough to support fast switching (AN1017, n.d.).

The bootstrap circuit consists of a capacitor and a diode and it has been widely used in low power gate drivers in order to reduce the number of isolated power supply in the voltage source inverter control circuitry (AN9035, n.d.; AN978, n.d.). Unfortunately this method is constrained by the need to refresh the bootstrap capacitor. In Klumpner et al. (2002) it is presented a three-phase matrix converter where part of the bi-directional power switches uses the common emitter

topology and the other part uses the common collector topology. This arrangement permits the use of bootstrap circuit so the number of isolated power supplies is reduced to three. However, with this approach is not possible to build three independent power modules. Moreover, the control of the matrix converter is more complex since that it must be assured that the bootstrap capacitor be charged during the start-up and also in the normal operation of the matrix converter.

Optocouplers with high common mode transient immunity have been commonly used to drive small and medium power IGBTs. Although this device needs an isolated power supply, it has a good performance over any PWM duty cycle so it was chosen to be used in this prototype.

The gate drive of each bi-directional switch uses two optocoupler gate drives (HCPL3140) and one isolated linear power supply as shown in Fig. 5. Although a low power flyback converter is a cost-effective solution to multiple isolated power supply, it was used linear power supplies in order to simplify the design of the power supplies and the layout of the printed circuit board. There was no need of negative voltage since low power IGBTs like IRGB15B60KD can be adequately turn-off using only positive gate drive. Three toroidal transformers provide the necessary isolation. Toroidal transformer has several advantages compared to laminated transformer like such as less volume, weight, and losses. Each toroidal transformer has four taps: three taps of 15 V to drive power supplies and one tap of 5 V to control circuitry.

An important IGBT parameter used to calculate the gate drive requirement is the gate capacitance charge. The gate capacitance influences the switching behavior of IGBTs like the switching time, switching losses, and short circuit capability. A gate resistor Rg, shown in Fig. 5, may control the gate capacitance charge. Taking into account the maximum peak output current of the HCPL3140 and the total gate charge required by the IRGB15B60KD, the minimum value of Rg can be determined according to the guideline given in HCPL3140/HCPL0314 datasheet. Rg is selected such that the maximum peak output current rating of the gate drive HCPL3140 is not exceeded. In this case, the peak current is 0.6 A . The Rg minimum (using Fig. 6 from hcpl3140 datasheet) is given by Rg $>$ (15-5)/0.6 = 16,67 Ω. However, in attempt to reduce the EMI problems, the gate resistor was increased to 22 Ω.

2.2 Safe commutation circuitry and protection

2.2.1 Implementation of a safe commutation

The proper switch commutation in the matrix converter requires that at any time only one bi-directional switch be conducting in each power module in order to avoid a short circuit or an overvoltage in the power bi-directional switches.

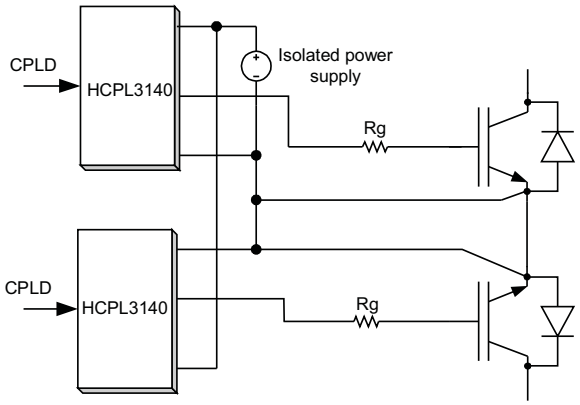


Figure 5: Gate drive of the bi-directional switches.

The strategy adopted to get safe commutation of the bi-directional switches is the four-step commutation scheme (Burany, 1989). This commutation scheme takes into account the load current sign and the state machine shown in Fig. 6. The Table 1, regarding the module shown in Fig. 4, gives the switching states. The states Saa, Sbb and Scc are the main states and represent the condition where the bi-directional switch is ready to conduct in both directions. The other states represent intermediate states during the commutation according to the safe commutation algorithm. Let us consider for example that the bi-directional switch formed by IGBTs Sa1 and Sa2, shown in Fig. 4, is conducting a current flowing from the voltage source Vi1 to the load (i $>$ 0) and the matrix converter must commute to the bi-directional switch formed by IGBTs Sc1 and Sc2. The commutations between the bi-directional switches according to the four-step scheme are given by the states sequence Saa$\rightarrow$S1$\rightarrow$S9$\rightarrow$S10$\rightarrow$Scc.

The implementation of the commutation process is an important issue not only for proper operation and safety of the matrix converter but also it must be completed in the smallest possible time in order to minimize the distortion on the output voltage (Kang et al., 2003).

The time necessary to complete a commutation sequence is responsible for a similar effect caused by the dead-time on the three-phase PWM inverter. Some modulation techniques like space vector modulation have a high number of commutations per sampling period making very difficulty to perform the implementation of state machine shown in Fig. 6 using a software approach.

On the other side, if the state machine is implemented using discrete components, it will demand many logical gates

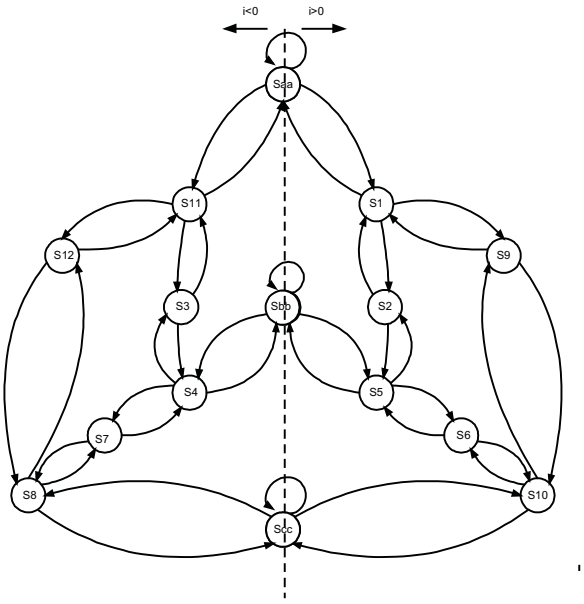


Figure 6: State transition diagram for safe commutation.

Table 1: Possible states of the IGBTs.

IGBT state						State
S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	Name
1	1	0	0	0	0	Saa
0	0	1	1	0	0	Sbb
0	0	0	0	1	1	Scc
1	0	0	0	0	0	S1
1	0	1	0	0	0	S2
0	1	0	1	0	0	S3
0	0	0	1	0	0	S4
0	0	1	0	0	0	S5
0	0	1	0	1	0	S6
0	0	0	1	0	1	S7
0	0	0	0	0	1	S8
1	0	0	0	1	0	S9
0	0	0	0	1	0	S10
0	1	0	0	0	0	S11
0	1	0	0	0	1	S12

and flip-flops making the commutation circuit large and complex. The best way to implement the commutation circuit is to use some kind of programmable logic device like as a CPLD (Complex Programmable Logic Device). The state machine in this case was implemented with three CPLDs XC9536, one CPLD for each power module. This CPLD is an in-system programmable device and the I/O pins can be configured for 3.3 V or 5 V operation and they can provide up to 24 mA output current which is sufficient to drive the HCPL 3140.

The CPLDs were configured using VHDL language (Very High Speed Integrated Circuit Hardware Description Language) (Dueck, 2000). VHDL is a hardware description language used to describe the behavior and structure of digital systems. In this design, each three phase to one phase matrix converter module (as shown in Fig. 4) has its own safe commutation controller, in this way, the signal commands from CPLD is very close to the HCPL3140. The XC9536 CPLD is the smallest CPLD from Xilinx with only 36 macrocells.

The CPLD receives and sends several signals. The input signals are: one bit from protection circuit for information of an short circuit occurrence, one bit from signal detector circuit for information about the load current sign and four bits from DSP where two bits inform about the input voltage source to be connected to the load, one bit is the start command, and one bit is used to reset the CPLD. The CPLD was set to operate at 2 MHz clock frequency, which provides a safe operating margin to drive the IGBT since that the turn-off delay time of the IGBT is about 230 ns. Timer 2 provides the clock signal to CPLD, so the operation of the CPLD is synchronized with operation of the DSP.

The output signals are: six signal commands, one to each gate drive in the power module, and one bit to DSP to indicate a short circuit condition.

Some care is necessary when using VHDL since the synthesis tool which implements the digital circuit described by VHDL code only accepts a subset of VHDL syntax and the resulting synthesis may be inefficient thus consuming many logic cells demanding a CPLD with more logic cells.

The first implementation of the state machine (shown in Fig. 6) consumed 46 macrocells. After several optimizations in the VHDL code, the number of macrocells reduced to 20 macrocells. The next XC9500 family is XC9572 with 72 macrocells, it is possible to implement all state machines for the three modules.

2.2.2 Load current signal detector circuit

The signal detection circuit consists of an LTS 6-NP current sensor, a second order low pass filter, and a zero crossing detector with hysteresis. The output of detection circuit is 5 V for a current flowing to load (i>0) and 0 V for a current flowing from load (I<0). The accuracy in the signal current detection is important for the correct operation of the commutation circuit. When the level of output current is near of zero current level, it is possible the occurrence of multiple

zero crossing due to the switching frequency ripple and the errors measurements. The measure range of LTS 6-NP sensor is ± 19 Apeak with a total accuracy of $\pm 0.2\%$ at 25°C which it suitable for this application. A second order low pass filter to attenuate the current ripple was designed using the Texas tool FilterPro^{TM}. The cut-off frequency is 4 kHz, slightly lower than the half of switching frequency to minimize the phase shift. Additional minimization of multiple zero crossing effects is got within the CPLD: the load current signal is kept constant during the intermediate states of the commutation process. Although it is difficulty to eliminate multiple zero crossing and the phase-shifts in the current signal measurements, the current level is small when it occurs and it doesn't cause any dangerous situation for matrix converter, besides the major commutations occur beyond this region.

2.2.3 Short-circuit protection

A line-to-line short circuit can occur if both bi-directional switches in the same power module are momentarily turned on due to any fault control/drive or induced noise malfunction. The IGBT IRGB15B60KD can support short-circuit for 10 μs, which can reach up to a peak current of 150 A. This characteristic is essential in the design of the short circuit protection circuit since the protection circuit presents a delayed action. Beside this, it is important to prevent an overload on power switching. For this, it was taking account that the current of IRGB15B60KD operating with a case temperature of 100°C which the collector current must be limited to 15 Arms. So, the current protection circuit was designed not only to deal with a short-circuit event but also to avoid overcurrent limiting the output current to 21 Apeak. The short-circuit protection is built with two Hall sensors LTS 25 NP with a measure range of ± 80 Apeak inserted in the phases Vi1 and Vi3, before the input filter. The detection of a short-circuit condition is implemented by using two windows comparators with LM 393 in an "OR" function. The levels of the windows comparator are ± 21 Apeak. When the short-circuit is detected, a 5 V signal is sent to all CPLDs which their response is a command to shutdown all IGBTs in each power modules. Since this process occurs in asynchronous mode the delay time is in the maximum of 0.5 μs for 2 MHz clock and the total response time of the Hall sensor and the analog circuit is about 4 μs, the estimated time to the current protection circuit to act is less than 5 μs.

2.2.4 Overvoltage protection

Since the IGBT must turn off very fast when a shutdown command occurs and do not exist a free wheeling path to the inductive load currents in the matrix converter, the collector-emitter voltage rises and the IGBT may be destroyed by overvoltage. Besides this, overvoltage may be produced by line disturbance in the input of the matrix converter. In order to avoid overvoltages, the switches of the matrix converter must be protected on both sides. The diode clamp circuit is a common solution to protect the matrix converter, as shown in Fig. 7, and it requires twelve fast diodes and one capacitor. The number of diodes may be reduced to at least six in a new clamp circuit as shown in Nielsen et al. (1999).

An alternative low cost solution for low power matrix converter is the use of MOVs (Metal Oxide Varistor) to protect the converter (Mahlein and Braun, 2000) and it was adopted here, as shown in Fig. 1. MOVs can respond to changes in voltage almost instantaneously for a properly selected device. It is important to connect the MOV with minimal lead length in order to minimize parasitic inductances that slow down the MOV response. Two parameters are important in the selection of the MOV: maximum clamp voltage and the absorb energy capability. For a 220 VRMS line voltage, the MOV S20K150 has an operating voltage of 240 VRMS and the maximum clamping voltage of 395 V. Since the selected IGBT supports a maximum collector-emitter voltage of 600 V, there is a good margin to safe protect IGBTs against overvoltage. For a three-phase RL load, the energy E to be absorbed may be calculated by

$$E = \frac{3}{4} L I^2 \tag{1}$$

where L is the load inductance and I is the rms current.

The maximum energy absorption capacity of S20K150 is 85 J during 2 ms. This value is enough to absorb the stored energy in the RL load used in the testes where L is 2 mH and Imax is 15 Arms. If the load is an AC motor, it is more complicated to calculate the energy stored in the magnetic circuit but some MOV manufacturers provide guidelines in selecting the appropriate MOV for this kind of load (Littelfuse, 2001).

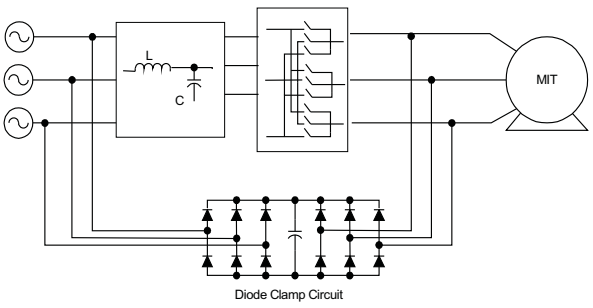


Figure 7: Overvoltage protection circuit using clamping diodes.

2.3 Modulation Techniques

The first modulation method for matrix converter presented by Venturini has the disadvantage to limit the matrix converter output rms voltage to 50% of the input rms voltage value, although it is very simple to implement. Several papers have been published showing different types of pulse width modulation schemes in order to increase the gain of output voltage (Accioly et al., 2007; Ribeiro et al., 1995; Huber and Borojevic, 1989; Mahlein et al., 1999; Alesina and Venturini, 1989). In (Alesina and Venturini, 1989) it was proved that for a three-phase to three-phase matrix converter the upper limit on the voltage ratio is 0.866 for any modulation method. Studies to reduce the output current riple was presented by Kim et al. (2010).

In this paper the space vector modulation method (section 2.3.2) to control the matrix converter is used due to its simplicity to perform the duty cycle calculation and due to the fact that it provides the maximum voltage gain of 0.866.

2.3.1 Venturini Modulation

In the converter control strategy proposed by Alesina and Venturini (1989), the average output voltage in each arm of the matrix converter is obtained from samples of input voltages. In Venturini modulation, each arm of the converter are switched sequentially within a sampling period T_a.

Considering only one arm of the matrix converter, in this case three-phase to one-phase, there are three switches in each interval sampling and the time intervals in each switching called t_a, t_b and t_c. The switching pattern of bidirectional switches S11, S21 and S31 of one arm of the matrix converter, by the strategy of the Venturini is shown in Figure 8.

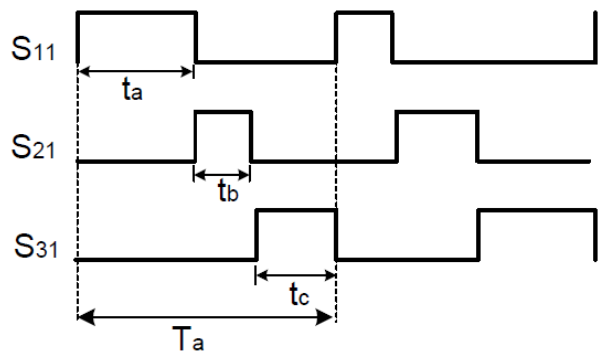


Figure 8: Switching sequence of Venturini modulation.

Thus, the output voltage of one arm of the matrix converter is given by

$$\overline{v}_{s1} = \frac{1}{T_a}\left[\overline{v}_{s1}(t)t_a + \overline{v}_{s2}(t)t_b + \overline{v}_{s3}(t)t_c\right] \tag{2}$$

and the duty cycles associated to the times t_a, t_b and t_c are given by:

$$m_a = \frac{t_a}{T_a} = \frac{1}{3} + \frac{2}{3}\frac{V_s}{V_e}\cos\left[\left(\omega_s - \omega_e\right)t\right] \tag{3}$$

$$m_b = \frac{t_b}{T_a} = \frac{1}{3} + \frac{2}{3}\frac{V_s}{V_e}\cos\left[\left(\omega_o - \omega_i\right)t + \frac{2\pi}{3}\right] \tag{4}$$

$$m_c = \frac{t_c}{T_a} = \frac{1}{3} + \frac{2}{3}\frac{V_s}{V_e}\cos\left[\left(\omega_o - \omega_i\right)t - \frac{2\pi}{3}\right] \tag{5}$$

Equation (2) allows synthesizing a three phase voltages system, for this, just use the Equation (3), but with angles of 120° and 240° degree.

This technique has the disadvantage to limit the matrix converter output *rms* voltage to 50% of the input *rms* voltage value, although it is very simple to implement.

2.3.2 The space vector PWM algorithm

The space vector modulation for matrix converter was first proposed in Huber and Borojevic (1989) where the matrix converter was modelled as a two-stage converter: a controlled rectifier stage and a voltage source inverter stage both connected via an imaginary dc link, as shown in Fig. 9. This approach permits to use the well-known space vector modulation method in both stages.

In the rectifier stage there are nine possible combinations that correspond to six active space vectors (I_1-I_6) and three zero vector (I_7-I_9). In the inverter stage, there are eight possible combination which produce six active vectors (V_1-V_6) and two zero vectors (V_7, V_8). Both active current vectors and active voltage vectors are shown in Fig. 10 and Table 2 describes them.

Using the subscripts a and b for the active input current vector that precedes and succeeds the input current reference vector i^* and the subscripts c and d for the active output voltage vectors that precedes and succeeds the output voltage reference vector v^*, and 0 for the zero current or voltage vector, a possible sequence of active input current vectors and active output voltage vectors to synthesized a sinusoidal output voltage and sinusoidal input current during a sampling interval Ts may be:

$$I_aV_c \rightarrow I_aV_d \rightarrow I_bV_d \rightarrow I_bV_c \rightarrow I_0V_0 \tag{6}$$

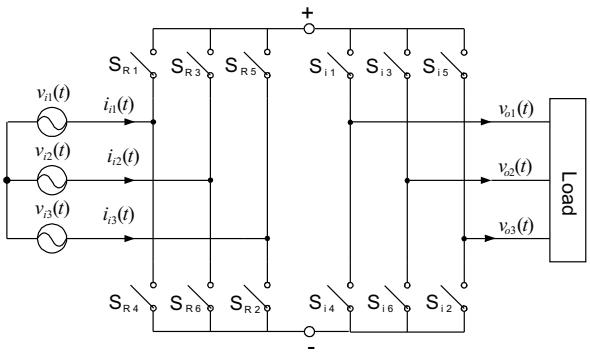


Figure 9: Matrix converter model for space vector modulation.

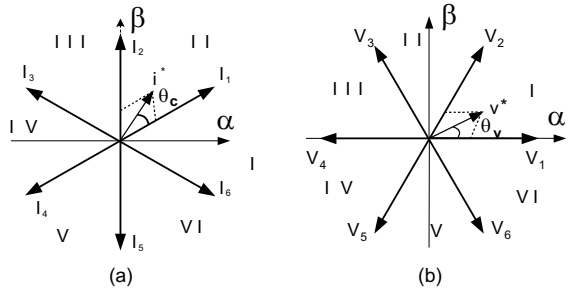


Figure 10: Space vectors in (a) Rectifier stage, (b) Inverter stage.

Table 2: Switch States.

Rectifier Stage		Inverter Stage	
Active Vector	Switch turned on	Active Vector	Switch turned on
$\mathbf{I_1}$	S_{R1}, S_{R2}	$\mathbf{V_1}$	S_{I1}, S_{I6}, S_{I2}
$\mathbf{I_2}$	S_{R2}, S_{R3}	$\mathbf{V_2}$	S_{I1}, S_{I3}, S_{I2}
$\mathbf{I_3}$	S_{R3}, S_{R4}	$\mathbf{V_3}$	S_{I4}, S_{I3}, S_{I2}
$\mathbf{I_4}$	S_{R4}, S_{R5}	$\mathbf{V_4}$	S_{I4}, S_{I3}, S_{I5}
$\mathbf{I_5}$	S_{R5}, S_{R6}	$\mathbf{V_5}$	S_{I4}, S_{I6}, S_{I5}
$\mathbf{I_6}$	S_{R6}, S_{R1}	$\mathbf{V_6}$	S_{I1}, S_{I6}, S_{I5}
$\mathbf{I_7}$	S_{R1}, S_{R4}	$\mathbf{V_7}$	S_{I1}, S_{I3}, S_{I5}
$\mathbf{I_8}$	S_{R3}, S_{R6}	$\mathbf{V_8}$	S_{I4}, S_{I6}, S_{I2}
$\mathbf{I_9}$	S_{R5}, S_{R2}	-	-

Consider, for example, the input current vector i* located in sector I and the output voltage v* located in sector III. So, the vector sequences are $I_6V_3 \rightarrow I_6V_4 \rightarrow I_1V_4 \rightarrow I_1V_3 \rightarrow I_0V_0$, with a=6, b=1, c=3, and d=4. Analyzing the vector pair I6V3, according to the table 2, the current vector I6 makes the voltage in the positive dc link to be v_{i1}(t) and in the negative dc link as v_{i2}(t). In the inverter side, the voltage vector V_3 implies the output voltages v_{o1}(t)= v_{i2}(t), v_{o2}(t)= v_{i1}(t), and v_{o3}(t)= v_{i2}(t). As any bi-directional switch of the matrix converter must perform both rectification and inversion simultaneously, the output voltages in the matrix converter must be v_{o1}(t)= v_{i2}(t), v_{o2}(t)= v_{i1}(t), and v_{o3}(t)= v_{i2}(t), as shown in Fig. 11(a). The states of the matrix converter for the space vector pairs are shown in Fig. 11.

The zero voltage and zero vectors are selected in order to minimize the switching in the matrix converter. So, for this example, the vectors I_9 e V_8 may be selected since they lead the matrix converter to execute only one commutation comparing with its early status.

2.3.3 Implementation on the DSP

The space vector algorithm was implemented on DSP TMS320F2812 with a sampling frequency of 10 kHz. This DSP has two event manager modules, named EVA and EVB that provide many resources to generate and manage events that are very useful in power converter control. Each event manager has two general-purpose timers: timers 1 and 2 for EVA and timers 3 and 4 for EVB. In this implementation of the space vector modulation, timer 1 period register (T1PR) is programmed to count 5000 times in order to generate the switching frequency of 10 kHz and it controls the time durations of current and voltage vectors, timer 2 generates the clock signal for all three CPLDs and it operates synchronized with timer 1 (both timer counters starts simultaneously), and timer 3 is used to generate the angle θ_c and θ_v.

The first task of the space vector program is to synchronize the input current reference vector with the input voltage vector. This synchronization is done using a zero crossing detector circuit connected to the input voltage v_{i1}(t). Since the input voltage is fixed in 60 Hz, the input current will be a 60 Hz waveform regardless the output voltage frequency. The angle θ_c is calculated by an integrator which it is initialized every time the DSP capture input pin detects a positive transitions in the zero crossing circuit. This procedure to synchronize the input current is enough if the input voltage is not distorted. If it is distorted, a PLL may be necessary. The output voltage angle θ_v is calculated by integration of the desired output voltage frequency. This frequency is given directly by the user using a window generated by the GEL files, a programming tool available in CodeComposer, and it is updated in real time. Both voltage and current integrators are implemented within of the interruption routine generated by timer 3 with a sampling frequency of 50 kHz, five times higher than switching frequency in order to get θ_c and θ_v with better precision. Then, the vector reference angles θ_c and θ_v are used to determinate the sector where the input current vector and the output voltage vector are located.

Now that the current and voltage sectors are known, the correct active and zero vectors must be synthesized. Using the procedure described previously to determine the active and zero vectors, there are 180 possible combinations of active and zero vectors. Each combination is coded in a six bits word length that is stored in a look-up table in the section data of the DSP. This 6 bits information are in fact three pair of bits that shows what input voltage each power module of the matrix converter must be connected at determined instant which "01" the power module must be connected to input voltage source V_{i1}, "10" to voltage source V_{i2} and "11" to voltage source V_{i3}. Considering the vector sequence $I_6V_3 \rightarrow I_6V_4 \rightarrow I_1V_4 \rightarrow I_1V_3 \rightarrow I_0V_0$ given previously. The data stored in the look-up table are: "100110", "100101", "110101", "110111", and "111111". The look-up table is organized so that its contend can be accessed y a pointer to an address given by:

$$\begin{aligned} \text{adress} = 5 * \text{output\_voltage\_sector} + \ldots \\ + 30 * \text{input\_current\_sector} \end{aligned} \tag{7}$$

The duty-cycles for each current and voltage vectors pairs given by (6) are calculated in the main routine according to (8) (Huber and Borojevic, 1989):

$$\begin{aligned} m_{ac} &= \text{int}\left(m.\sin\left(60^\circ - \theta_c\right).\sin\left(60^\circ - \theta_v\right).5000\right) \\ m_{ad} &= \text{int}\left(m.\sin\left(60^\circ - \theta_c\right).\sin\left(\theta_v\right).5000\right) \\ m_{bd} &= \text{int}\left(m.\sin\left(\theta_c\right).\sin\left(60^\circ - \theta_v\right).5000\right) \\ m_{bc} &= \text{int}\left(m.\sin\left(\theta_c\right).\sin\left(60^\circ - \theta_v\right).5000\right) \end{aligned} \tag{8}$$

where: m is the modulation index, θ_c is the current vector reference angle and θ_v is the voltage vector reference angle, both shown in Fig. 10.

The calculated duty cycles are stored in four compare register from timer 1 named CMPR1, CMPR2, CMPR3, and T1CMPR, as shown in Fig. 12, where each comparator register generates an interruption. One can see that the zero vector pair I0V0 is implicitly generated by T1PR. So, during each duty cycle interval the DSP is always sending to each CPLD the information of which input voltage phase the matrix converter must connect to the load. The initial pointer address is calculated only in the interrupt routine generated by the T1PR register and it is incremented in the next interruptions routines generated by the other compare register.

Since the space vector modulation is somewhat complex to implement, it may be interesting to test the implemented algorithm in real time before apply it in the control of the matrix converter. A simple way to test the space vector modulation is to build an analog simulator as shown in the block diagram of Fig. 13. It consists of a 120 degree shifter built with operational amplifier, nine CMOS 74HC4316 bilateral switches to simulate the bi-directional matrix converter switches and three low pass filters to simulate the inductive load.

In Fig. 14 it is shown an experimental result using the analog simulator in order to test the space vector algorithm implemented on the DSP where channel 3 shows the output line voltage and the channel 1 shows the filtered output voltage. More complicated algorithms to control the matrix converter can be implemented and tested without risks for example an algorithm to compensate input voltage distortion.

In the space vector modulation technique there is a scattering of the harmonic components in the spectrum of switching frequency while in the technique Venturini, the modulation of the harmonic components are well defined around multiple of the switching frequency as can be seen in Figures 14(b) and 14(c). Also important is the fact that the amplitude of the fundamental components of voltage and current are comparatively higher compared to those presented in the Venturini modulation technique, which is limited to a maximum voltage gain of 0.5.

2.4 Input filter design

Due to the fact that the matrix converter acts as a current source converter for the electrical power source, an input filter is necessary to filter the high frequencies ripple present in the input currents.

There are several constraints that it must take into account in the input filter design: cost, volume, and switching noise attenuation are some of them. The input filter described here is a single stage damped LC filter and its design aims to maximize the input displacement factor (IDF) (Zargari et al., 1994; Vlatkovic et al., 1996). Since the capacitor is the main responsible for reducing the IDF, the capacitor value must be minimized. In Vlatkovic et al. (1996), the upper limit for the capacitor value is given by:

$$C_{max} = \frac{I_m}{\omega V_m} \tan\left(\cos^{-1} IDF\right) \tag{9}$$

where: I_m is the maximum input current, V_m is the maximum input voltage and ω is the angular frequency of the input voltage.

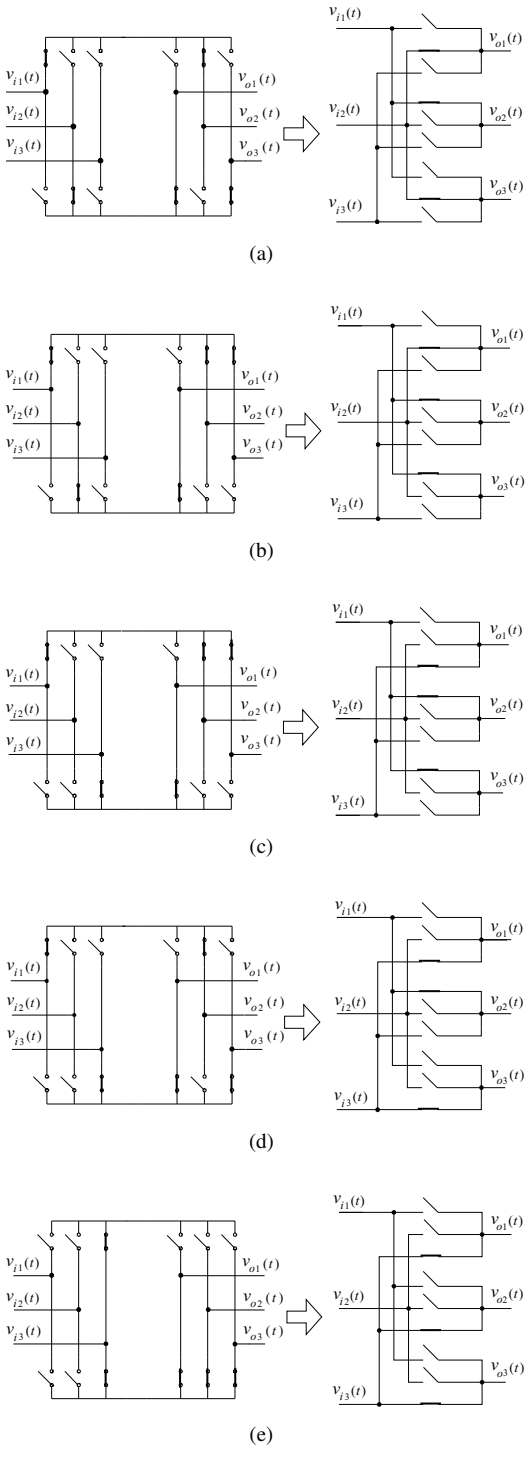


Figure 11: Matrix converter switching sequence.

The damping resistor Rd and the inductor L can be calculated using the harmonic equivalent model of the input filter shown in Fig. 15.

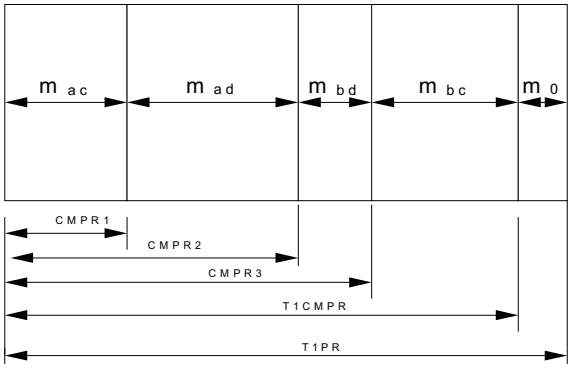


Figure 12: Switching sequence for space vector modulation.

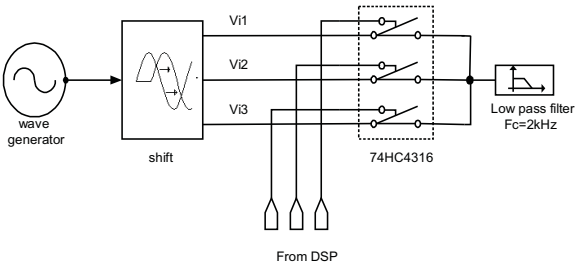


Figure 13: Analog three-phase to one-phase matrix converter simulator.

The transfer function $G(s)$ of the filter is:

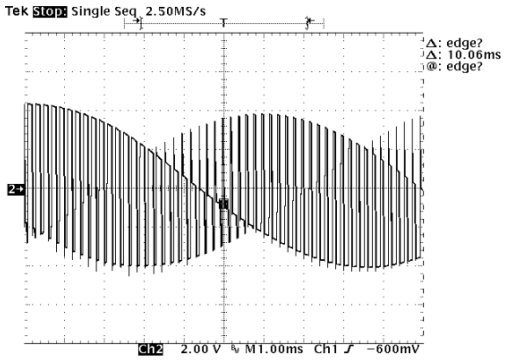
$$G(s) = \frac{I_{L,h}}{I_{mc,h}} = \frac{1 + sR_dC}{s^2LC + sR_dC + 1} = \frac{\frac{1}{LC} + s\left(\frac{R_d}{L}\right)}{s^2 + s\left(\frac{R_d}{L}\right) + \frac{1}{LC}} \quad (10)$$

The damping ratio ξ and the natural angular frequency ω_n of the filter are given by (11) and (12):

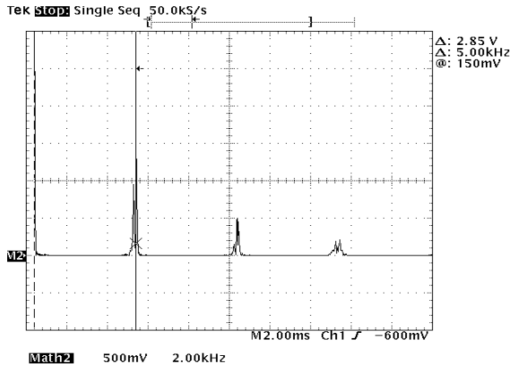
$$\xi = \frac{R_d}{2\omega_n L} = \frac{R_d}{2}\sqrt{\frac{C}{L}} \quad (11)$$

$$\omega_n = \frac{1}{\sqrt{LC}} \quad (12)$$

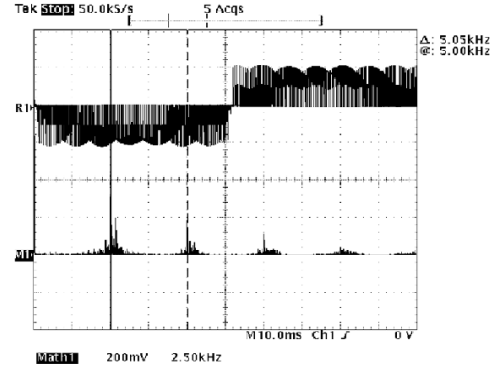
Taking into account that maximum power of the prototype in this work is 2 kW, the maximum input current is limited to 5 A for 220 voltage three-phase power supply. Using (9), the maximum capacitance C for the input filter is approximately 15 μF. Connecting the capacitors in delta, this value decreases to 5 μF. According to Adelson and Farr (1985),



(a) Phase voltage of Venturini modulation.



(b) FFT of phase voltage of Venturini modulation.



(c) Phase voltage and its FFT of space vector modulation.

Figure 14: Experimental result with the analog matrix converter simulator.

polypropylene film capacitors are the best choice for this application.

The inductance L may be calculated using (12) for a chosen ω_n. However, there were available in the laboratory several 250 μH toroidal inductors with powdered iron core and they were used in the filter. The damping resistor R_d was calculated using (11) and it was considered the damping ratio

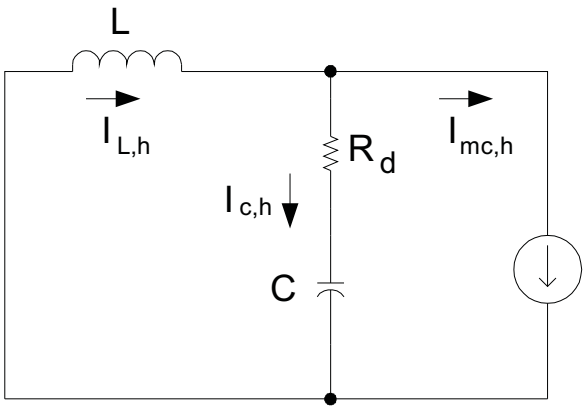


Figure 15: Input filter model.

$\xi = 0.25$ which results $R_d = 2.5\ \Omega$. Using delta connection this value is increased to 7.5 Ω.

In Fig. 16 it is shown the attenuation characteristic of the designed filter:

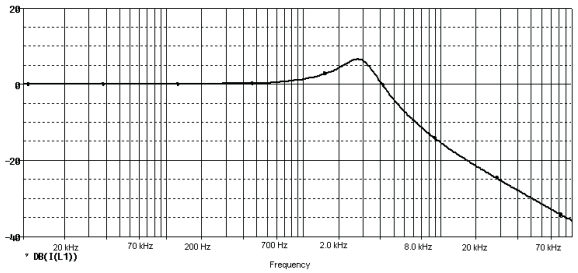


Figure 16: Attenuation characteristic of the input filter.

The filter looses can be improved if instead of use a damping resistor, an active damping scheme is implemented in the control (Sato and Kataoka, 1996).

2.5 Simulation Results

Some simulations of the matrix converter were done using Simulink. The switching frequency is 10 kHz and the matrix converter is feeding a three-phase Y-connected RL load with $R = 13\ \Omega$ and $L = 2\ mH$ and the input voltage is 220 V.

In Fig. 17 is shown the input current without filtering. In this condition, the input current is highly distorted by high frequency components generated by the switching of the converter. These high frequency components may cause malfunction on sensible equipments and must be attenuated by an input filter. Applying the filter designed previously in simulation, the high frequencies components are attenuated and the Total Harmonic Distortion (THD) of the input current is

reduced to about 5%, as shown in Fig. 18. However the designed filter produces a small displacement between the input voltage and current with IDF approximately of 0.98 as shown in Fig. 19. This displacement can be reduced if smaller capacitors are used, but this will degraded the filter capability.

The output voltage and current are shown in Fig. 20 and Fig. 21 respectively. One can see that the output current frequency on matrix converter is independent of AC mains.

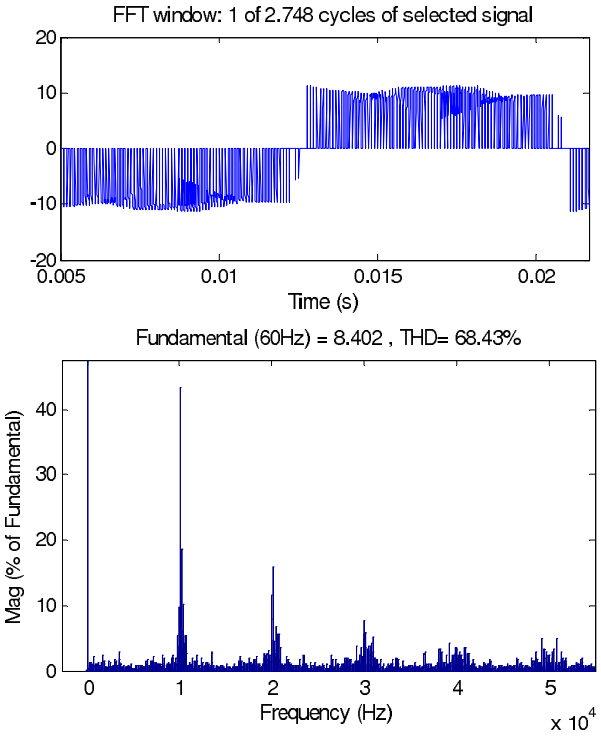


Figure 17: Non-filtered input current.

3 EXPERIMENTAL RESULTS

Some experimental results of the matrix converter prototype feeding a three-phase Y-connected RL load with $R = 13\ \Omega$ and $L = 2\ mH$ are shown in next figures. The input voltage are provided by a three-phase variac and the modulation index is 0.9. In Fig. 22 it is shown the input voltage v_{i1} and the filtered input current. One can see that the input current is slightly advanced from the input voltage. This is because the matrix converter is operating below the operating point, which the filter was designed to give the power factor close to one but the input current displacement is very close to the simulated result showed in Fig. 19. Beside this, the input voltage at output of variac is slightly distorted which cause some degree of distortion on output voltage and input current, since any strategy was used to eliminate the input voltage distortion. In Fig. 23 is shown the output voltage and its harmonic spectrum when the output frequency is fixed in

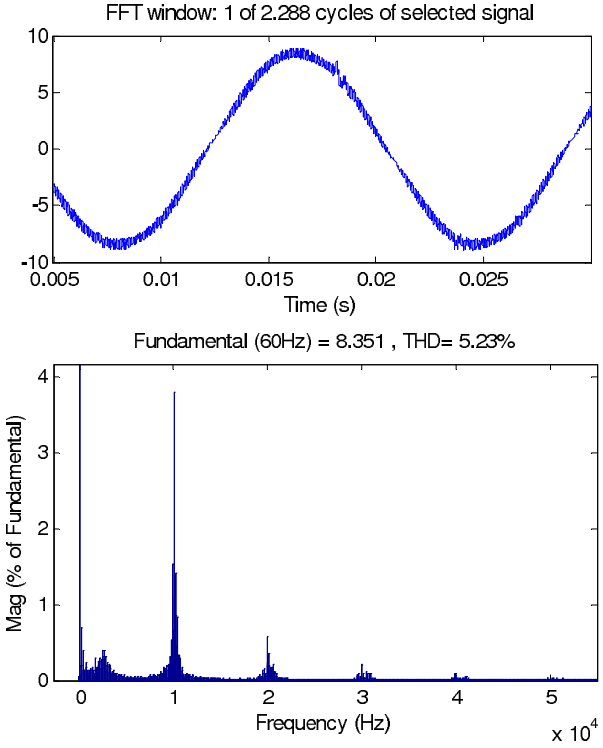


Figure 18: Filtered input current.

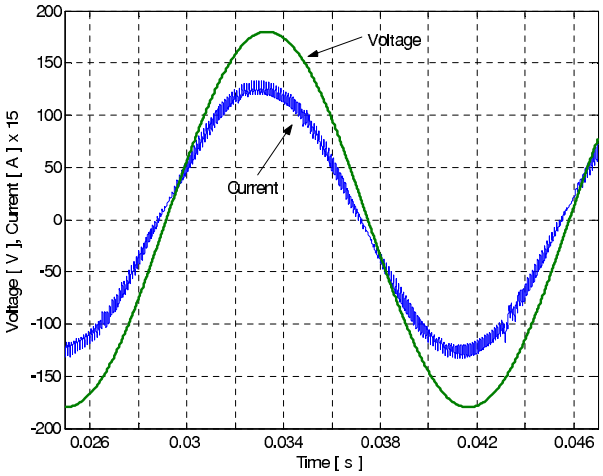


Figure 19: Input line voltage and input current displacement.

40 Hz. The output current for 40 Hz is shown in Fig. 24. These results are very close to the simulated results shown in Fig. 20 and Fig. 21. New acquisition was done to verify the prototype matrix converter performance operating with an output voltage frequency as low as 20 Hz and as high as 100 Hz output voltages, which is above the input voltage frequency. The output line voltage and output current are shown from Fig. 25 to Fig. 28. These results show that, although limited, the matrix converter prototype can operate well with

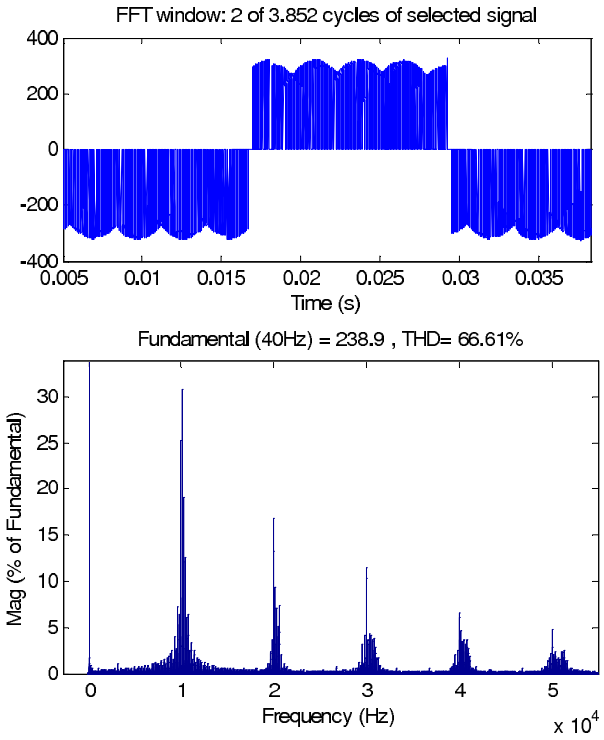


Figure 20: Output line voltage.

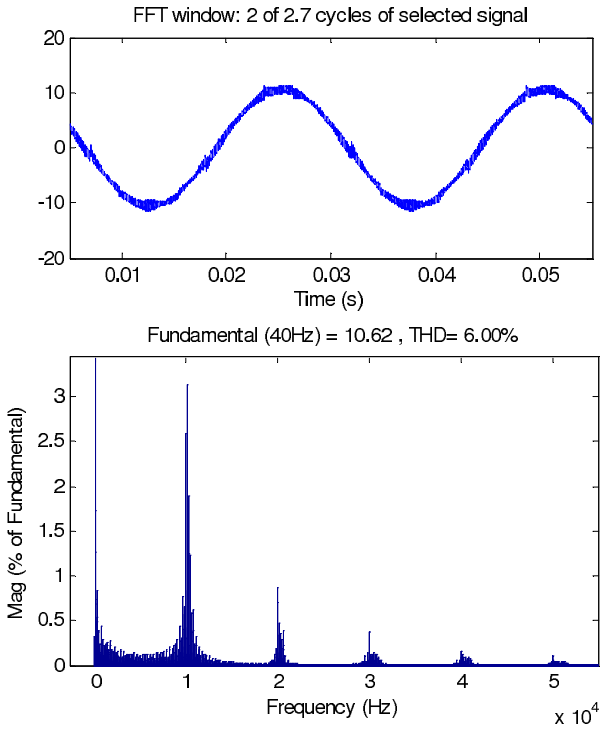


Figure 21: Output current.

output voltage frequencies below and above the power supply frequency (60 Hz).

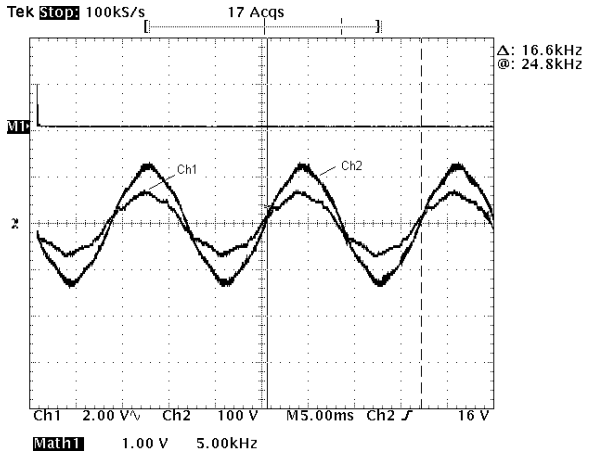


Figure 22: CH1: input current, CH2: input voltage.

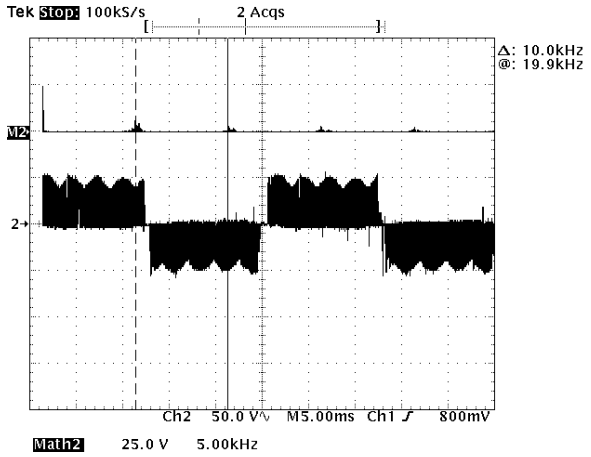


Figure 23: Output line voltage (40 Hz) and its harmonic spectrum.

4 CONCLUSION

This paper presents several design aspects of a low power matrix converter prototype and experimental results. The presented design of the matrix converter is based on components that are fairly easy to find in the marked. Besides this, it is suggested a simple analog matrix converter simulator, which may be very useful to develop new modulation algorithms for matrix converter.

ACKNOWLEDGEMENT

The authors would like to thank FAPESP - Fundao de Amparo Pesquisa do Estado de So Paulo, CAPES and CNPq -

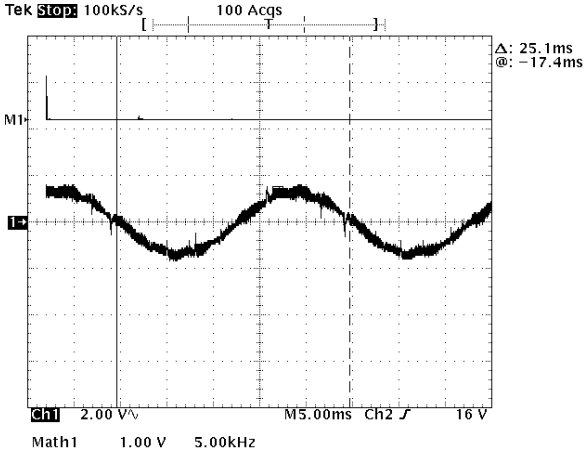


Figure 24: Output current (40 Hz) and its harmonic spectrum.

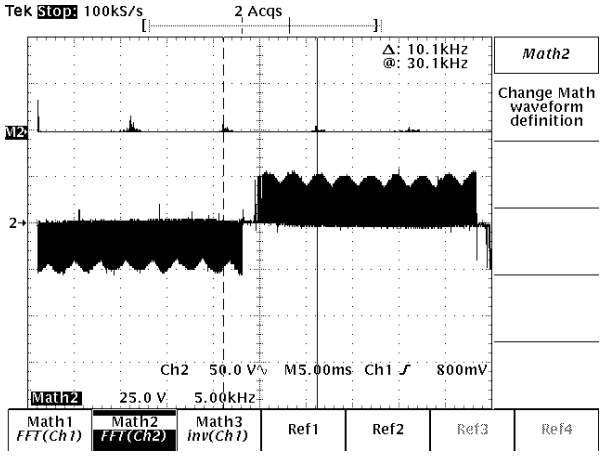


Figure 25: Output line voltage (20 Hz) and its harmonic spectrum.

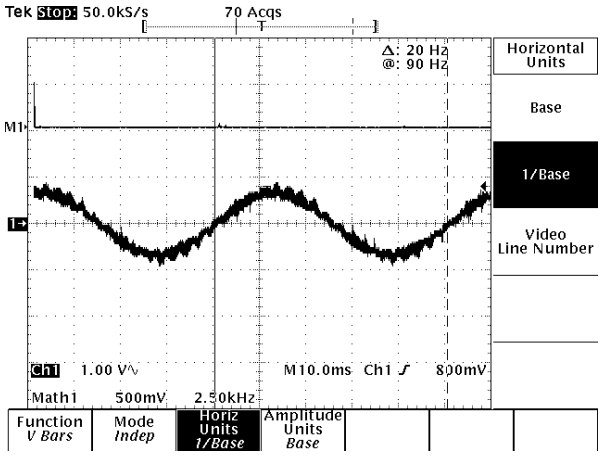


Figure 26: Output current (20 Hz) and its harmonic spectrum.

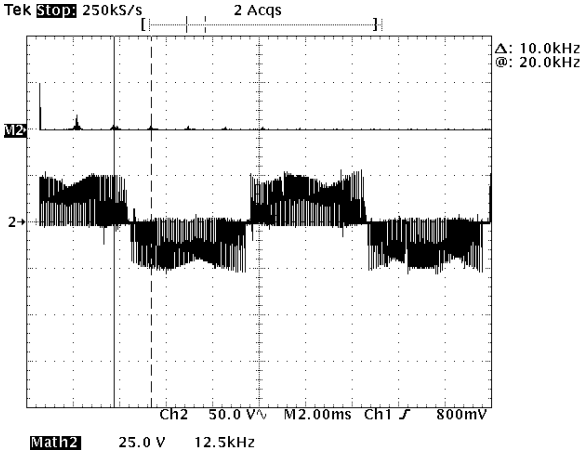


Figure 27: Output voltage (100 Hz) and its harmonic spectrum.

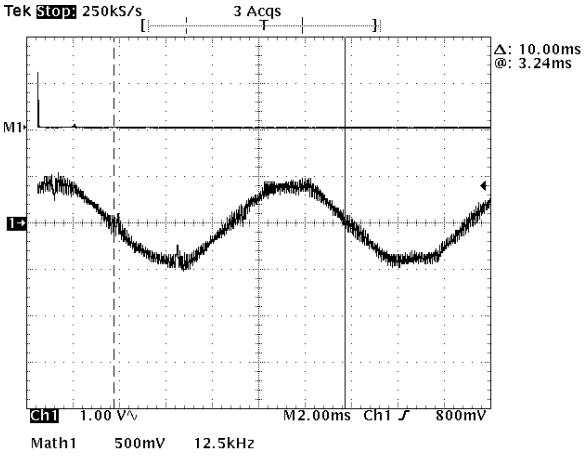


Figure 28: Output current (100 Hz) and its harmonic spectrum.

for the financial support for this research and also to Texas Instruments for the DSP evaluation board donation.

REFERENCES

Accioly, A., Lima, V., Bradaschia, F., Neves, F., Cavalcanti, M. and Samuel Neto, A. (2007). Scalar pulse width modulation strategies for matrix converter, *Eletrnica de Potncia* **12**: 53–62.

Adamek, J., Hofmann, W. and Ziegler, M. (2003). Fast commutation process and demand of bidirectional switches in matrix converters, *IEEE 34th Annual Power Electronics Specialist Conference, 2003. PESC '03.*, Vol. 3, pp. 1281–1286.

Adelson, L. and Farr, H. (1985). Polypropylene-film capacitors for military and industrial a-c applications. Appli-

cation notes, Dearborn Electronics, Inc.

Alesina, A. and Venturini, M. (1989). Analysis and design of optimum-amplitude nine-switch direct ac-ac converters, *IEEE Transactions on Power Electronics* **4**(1): 101–112.

AN1017 (n.d.). The pvi - a new versatile circuit element. International Rectifier, Application Note.

AN9035 (n.d.). Smart power module module. Fairchild Semiconductor, Application Note.

AN978 (n.d.). Hv floating mos-gate drivers ics. International Rectifier, Application Note.

Burany, N. (1989). Safe control of four-quadrant switches, *Conference Record of the 1989 IEEE Industry Applications Society Annual Meeting, 1989.*, Vol. 1, pp. 1190–1194.

Cha, H. and Enjeti, P. (2004). Matrix converter-fed asds, *IEEE Industry Applications Magazine* **10**(4): 33–39.

Dueck, R. (2000). *Digital Design with CPLD Applications and VHDL*, Thomson Delmar Learning.

Gabe, I., Massing, J., Montagner, V., Grigoletto, F. and Pinheiro, H. (2009). Projeto e implementao de um controlador de corrente robusto para inversores com filtro lcl conectados rede com incertezas paramtricas, *SBA Controle & Automao* **20**(1): 94–104.

Gyugyi, L. and Pelly, B. (1976). *Static Power Frequency Changers - Teory, Performance and Applications*, John Willey and Sons.

Huber, L. and Borojevic, D. (1989). Space vector modulator for forced commutated cycloconverters, *Conference Record of the IEEE Industry Applications Society Annual Meeting, 1989.*, pp. 871 –876 vol.1.

Kang, J.-K., Hara, H., Yamamoto, E., Swamy, M. and Kume, T. (2003). Output voltage distortion in matrix converter by commutation of bi-directional switches, *IEEE International Electric Machines and Drives Conference, 2003. IEMDC'03.*, Vol. 1, pp. 55–59.

Khwan-on, S., De Lillo, L., Empringham, L. and Wheeler, P. (2010). A fault tolerant matrix converter motor drive under open phase faults, *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, pp. 1–6.

Kim, S., Yoon, Y.-D. and Sul, S.-K. (2010). Pulsewidth modulation method of matrix converter for reducing output current ripple, *IEEE Transactions on Power Electronics* **25**(10): 2620–2629.

Klumpner, C., Nielsen, P., Boldea, I. and Blaabjerg, F. (2002). A new matrix converter motor (mcm) for industry applications, *IEEE Transactions on Industrial Electronics* **49**(2): 325–335.

Lee, K.-B. and Blaabjerg, F. (2005). A nonlinearity compensation method for a matrix converter drive, *IEEE Power Electronics Letters* **3**(1): 19–23.

Littelfuse (2001). Application note ec638 - littelfuse varistor design example, `http://www.littelfuse.com/data/en/Application_Notes/EC638.pdf`.

Mahlein, J. and Braun, M. (2000). A matrix converter without diode clamped over-voltage protection, *The Third International Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000.*, Vol. 2, pp. 817–822.

Mahlein, J., Simon, O. and Braun, M. (1999). A matrix converter with space vector control enabling overmodulation, *8th European Conference Power Electronics and Applications*.

Michels, L., Camargo, R., Botteron, F. and Pinheiro, H. (2005). Metodologia de projeto de filtros de segunda ordem para inversores de tenso com modulao pwm digital, *SBA Controle & Automao* **6**(2): 221–242.

Mohite, S. and Gujarathi, P. (2010). A design and implementation of a novel multimode single phase matrix converter, *International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010*, pp. 1227–1230.

Nielsen, P., Blaabjerg, F. and Pedersen, J. (1999). New protection issues of a matrix converter: design considerations for adjustable-speed drives, *IEEE Transactions on Industry Applications* **35**(5): 1150–1161.

Pomilio, J. (2006). Dimensionamento de sistemas de dissipao de calor para dispositivos semicondutores, Apostila do curso de eletrnica de potncia - FEEC - UNICAMP.

Ribeiro, E., Roy, G. and April, G.-E. (1995). The implementation of a dfc topology under scalar control algorithm with a voltage gain beyond unity, *Proceedings of the IEEE International Symposium on Industrial Electronics, 1995. ISIE '95.*, Vol. 2, pp. 485–490.

Saengseethong, A. and Sangwongwanich, S. (2010). A new modulation strategy for capacitor voltage balancing in three-level npc inverters based on matrix converter theory, *International Power Electronics Conference (IPEC), 2010*, pp. 2358–2365.

Sato, Y. and Kataoka, T. (1996). A current-type pwm rectifier with active damping function, *IEEE Transactions on Industry Applications* **32**(3): 533–541.

Simon, O., Mahlein, J., Muenzer, M. and Bruckmarm, M. (2002). Modern solutions for industrial matrix-converter applications, *IEEE Transactions on Industrial Electronics* **49**(2): 401–406.

Sokolovs, A. and Galkin, I. (2008). Cost and space effective igbt gate drive circuit for bi-directional switch of matrix converter, *11th International Biennial Baltic Electronics Conference, 2008. BEC 2008.*, pp. 293–296.

Takei, M., Naito, T. and Ueno, K. (2003). The reverse blocking igbt for matrix converter with ultra-thin wafer technology, *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, pp. 156 – 159.

Venturini, M. (1980). A new sine wave in, sine wave out conversion technique eliminates reactive elements, *Proc. Powercon* **7**: 1–15.

Vlatkovic, V., Borojevic, D. and Lee, F. (1996). Input filter design for power factor correction circuits, *IEEE Transactions on Power Electronics* **11**(1): 199–205.

Wang, Q., Chen, X. and Ji, Y. (2010). The control of matrix converter ac excited brushless double-fed wind power unit, *Power and Energy Engineering Conference (APPEEC), 2010 Asia-Pacific*, pp. 1–5.

Wheeler, P., Clare, J., Katsis, D., Empringham, L., Bland, M. and Podlesak, T. (2004). Design and construction of a 150 kva matrix converter induction motor drive, *Second International Conference on (Conf. Publ. No. 498) Power Electronics, Machines and Drives, 2004. (PEMD 2004).*, Vol. 2, pp. 719–723.

Xie, Y. and Ren, Y. (2004). Implementation of dsp-based three-phase ac-ac matrix converter, *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, Vol. 2, pp. 843 – 847 vol.2.

Zargari, N., Joos, G. and Ziogas, P. (1994). Input filter design for pwm current-source rectifiers, *IEEE Transactions on Industry Applications* **30**(6): 1573–1579.