

Hot Electron Transport Properties in Characteristics of Wurtzite GaN MESFETs Using a Five-valley Model

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Ensemble Monte Carlo simulations have been carried out to investigate the effects of upper valleys on the characteristics of wurtzite GaN MESFETs. Electronic states within the conduction band valleys at the Γ_1 , U , M , Γ_3 and K are represented by non-parabolic ellipsoidal valleys centred on important symmetry points of the Brillouin zone. The following scattering mechanisms, i.e., impurity, polar optical phonon, acoustic phonon, alloy and piezoelectric are included in the calculation. Ionized impurity scattering has been treated beyond the Born approximation using the phase-shift analysis. The simulation results show that on the drain side of the gate region, hot electrons attained enough energy to be scattered into the upper satellite conduction valleys. Approximately 20% of the electrons occupy the higher valleys (mainly U and M valley). The simulated device geometries and doping are matched to the nominal parameters described for the experimental structures as closely as possible, and the predicted drain current and other electrical characteristics for the simulated device including upper valleys show much closer agreement with the available experimental data.

Keywords: Monte Carlo; Ellipsoidal valleys; Ionized impurity; Phase-shift

1. INTRODUCTION

GaN has become an attractive material for power transistors due to its wide band gap, high breakdown electric field strength, and high thermal conductivity [1-3]. Also the material has a relatively high electron saturation drift velocity and low relative permittivity, implying potential for high frequency performance [4-5]. Due to its wide band gap, GaN is a primary candidate for optoelectronic devices operating with blue to ultraviolet wavelengths and electronic devices operating at high temperatures and high power levels [6]. Several GaN-based transistors, superlattices, and quantum well devices intended for both electronic and optoelectronic applications [7-8]. Improved electron transport properties are one of the main targets in the ongoing study of GaN material and devices. It is considered reasonably well established that the electron drift velocity dependence on electric field has a region of negative differential conductivity. The electron drift velocity is predicted to have a maximum of $\sim 2.3 \times 10^5 \text{ ms}^{-1}$ at $\sim 2 \times 10^7 \text{ Vm}^{-1}$ for $T=300 \text{ K}$ and with an impurity concentration of about 10^{22} m^{-3} [9]. The velocity-electric field dependence exhibits remarkable thermal stability between 300 and 600 K.

In this work an ensemble Monte Carlo calculations of steady state electron transport in wurtzite GaN based field effect transistor has been presented. In next section, details of the device fabrication and simulation model which is used in the characteristic of the device are presented. Details of the effects of upper valley in GaN MESFETs and the results obtained are interpreted in section 3.

2. MODEL, DEVICE AND SIMULATIONS

An ensemble Monte Carlo simulation have been carried out to simulate the electron transport properties in wurtzite

GaN MESFET. The method simulate the motion of charge carriers through the device by following the progress of 10^4 superparticles. These particles are propagated classically between collisions according to their velocity, effective mass and the prevailing field. The selection of the propagation time, scattering mechanism and other related quantities is achieved by generating random numbers and using this numbers to select, for example, a scattering mechanism. Our self-consistent Monte Carlo simulation was performed using an analytical band structure model consisting of five non-parabolic ellipsoidal valleys. The pseudopotential band structure shows the conduction band minimum to be located at the Γ point (Γ_1), and lowest energy conduction band satellite valleys to occur at the U point (located about two thirds of the way between the L and M symmetry points). Higher conduction band valleys are located at the Γ point (Γ_3), at the M point, and at the K point (figure 1).

In our Monte Carlo simulation, the two different Γ valleys, the six equivalent U valleys, the three equivalent M valleys and the two equivalent K valleys are represented by ellipsoidal, non-parabolic dispersion relationships of the following form [10-11]

$$E(\mathbf{k})[1 + \alpha_i E(\mathbf{k})] = \frac{\hbar^2}{2} \left[\frac{k_x^2 + k_y^2}{m_{\perp}^*} + \frac{k_z^2}{m_{\parallel}^*} \right] \quad (1)$$

where m_{\perp}^* and m_{\parallel}^* are the transverse and longitudinal effective masses at the band edge and α_i is the non-parabolicity coefficient of the i -th valley. Scattering mechanisms included in the simulation are acoustic deformation potential, piezoelectric, alloy and ionised impurity scattering. Elastic ionised impurity scattering is described using the screened Coulomb potential of the Brooks-Herring model. Furthermore, longitudinal optical phonon scattering, nonequivalent and, where applicable, equivalent intervalley scattering events are taken into account among all valley types with the transfers assumed to be governed by the same deformation potential fields and the same phonon frequencies. Degeneracy effects are expected to be negligible over almost all of the temperature and electron concentration ranges of interest here and, hence, are not considered in the calculation.

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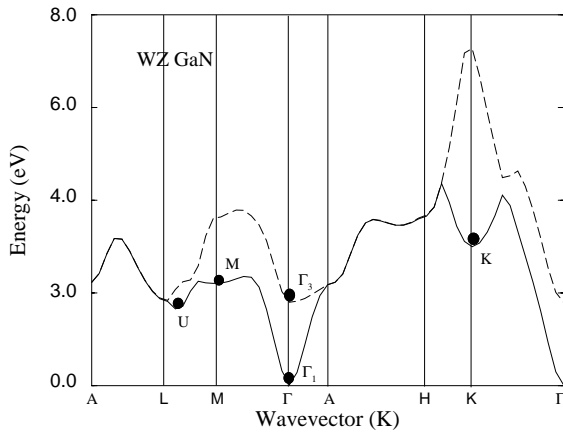


FIG. 1: Five-valley model of the two lowest conduction bands of wurtzite GaN used in the Monte Carlo simulations.

Electron particles in the ensemble Monte Carlo simulation occupy non-parabolic ellipsoidal valleys in reciprocal space, and obey Boltzmann statistics. Herring-vogt transformations are used to map carrier momenta into spherical valleys when particles are drifted or scattered. The electric field equations are solved self-consistently with the electron transport using a finite difference method, and the device grid potentials are updated at each ensemble drift timestep (1 femtosecond). The geometry of the device to be simulated is specified at the beginning of the simulation by defining it in an $x-y$ plane as a set of joined rectangular regions, each with uniform doping and other material parameters, and a set of contact regions. All physical quantities are assumed constant in the z direction (device width).

Figure 2 shows a simple example of joined rectangular regions and contacts for a MESFET structure. The solution of Poisson's equation is based on a finite difference method which requires that all the rectangular regions of the device are divided into uniform arrays of two-dimensional mesh cells. The cells may differ in form from region to region but it is necessary that they match in size along the join between two adjacent regions.

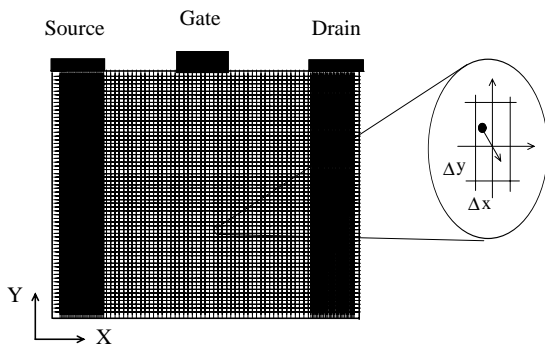


FIG. 2: Device geometry and discretization of a MESFET. There are three regions and three contacts S, G and D. The mesh cells are uniform within any single region and match at the joins.

In figure 2 the rectangular source and drain regions have identical uniform mesh cells which are different from those

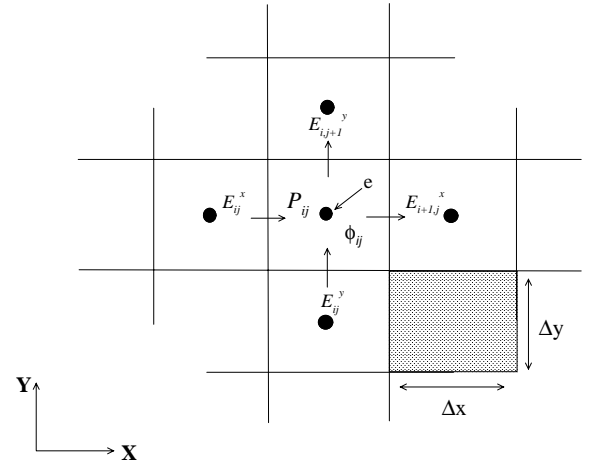


FIG. 3: Nearest-grid-point method for charge assignment in two-dimensions. The charge density at a mesh point P_{ij} is taken to be the total charge in the mesh cell surrounding the mesh point P_{ij} divided by the cell area. Note discretized electric field E_{ij} and electric potential ϕ_{ij} , ($E = -\nabla\phi$) are used in the solution of Poisson's equation.

in gate region, but match at the joins. The cells also form the frame of reference in which the particles move under the influence of the electric field. The definition of the mesh (shape and size of the cells) is dependent on the details of the device and the simulation, since, for example, the resolution of the electric field is limited by the size of the mesh cells.

The simplest method for assigning charged particles to cells is the nearest-grid-point scheme in which the total charge found in a cell is assigned to the midpoint of that cell (figure 3). After each sampling Poisson's equation is solved and the electric field is updated. Poisson's equation is solved by a combined fast Fourier transform [12-13] and Buneman cyclic reduction method [14] developed by Walmley and Abram [15]. This calculational scheme is integrated with a capacity matrix approach [16] that facilitates the use of individual rectangular regions to form more complicated structures.

After setting all the material and device parameters, the simulation is started in a state of charge neutrality everywhere in the device. The simulated particles are distributed appropriately among all the mesh cells to achieve the required neutrality. In the two-dimensional device models used here there is no variation of electron density or electric field normal to the $x-y$ plane and scalar quantities at a timestep like electron density, energy and potential are located at the center of the cells, whereas vectorial quantities like the electric field components or the velocity components are always calculated first at midpoint between the scalar quantities.

The particles that leave cell (i,j) in x -direction enter cell $(i+1,j)$ and analogously for the y -direction. Therefore, the total number of electrons in the simulated transistor can only be changed at the boundary of the simulation regions.

The device structure illustrated in figure 4 is used in all the simulations. The overall device length is $3.3 \mu\text{m}$ in the x -direction and the device has a $0.3 \mu\text{m}$ gate length and $0.5 \mu\text{m}$ source and drain length. The source and drain have ohmic contacts and gate is in Shottky contact in 1 eV to rephere-

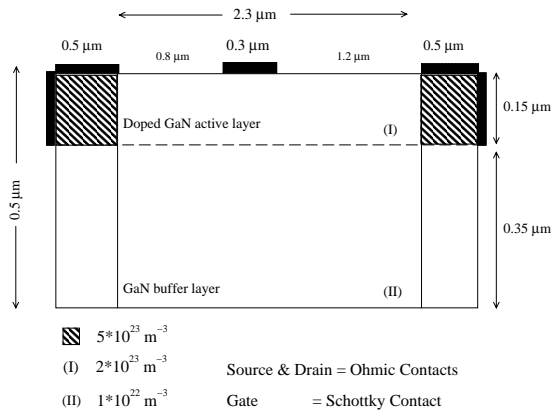


FIG. 4: Cross section of wurtzite GaN MESFET structure which we have chosen in our simulation. Source and drain contacts have low resistance ohmic contacts, while the gate contact forms a Schottky barrier between the metal and the semiconductor epilayer.

sent the contact potential at the Au/Pt. The source and drain regions are doped to $5 \times 10^{23} \text{ m}^{-3}$ and the top and down buffer layers are doped to $2 \times 10^{23} \text{ m}^{-3}$ and $1 \times 10^{22} \text{ m}^{-3}$, respectively. The effective source to gate and gate to drain separation are $0.8 \mu\text{m}$ and $1.2 \mu\text{m}$, respectively. The large dimensions of the device need a long simulation times to ensure convergence of the simulator.

3. RESULTS

Figure 5 compares the instantaneous distribution of electrons throughout the device in the steady-state for different gate and drain biases at room temperature. When a positive potential V_{ds} is applied to the drain, electrons flow from source to drain, giving a current I_{ds} from source to drain. The depletion region of the Schottky barrier restricts the current path to the lower part of the channel and the buffer layer. At zero drain bias (figure 5a), the depletion layer beneath the gate has a symmetric shape. At zero gate and drain bias, the depletion region corresponds to that associated with the built-in potential of the Schottky barrier, but is larger for the case of gate bias $V_{gs} = -1 \text{ V}$ shown here. As V_{ds} is increased from zero, the depletion layer becomes asymmetric in shape since the potential difference between the gate and the channel is greater at the drain end than the source end of the gate. The channel is more constricted at the drain end of the gate (see for example at $V_d = 18$ and 30 volt in figures 5b and 5c) and the field along the channel is also higher in that region.

As the drain-source voltage is increased still further, the field at the drain end of the gate approaches the value at which the electron velocity along the channel saturates. Beyond this value, which corresponds to the threshold voltage in the drain current-voltage characteristics, further increase in drain-source voltage does not substantially increase the drain-source current. The length of the region of the channel over which the electrons are in velocity saturation increases and there is some carrier accumulation within the channel. The depletion layer edge at the drain end of the gate also moves closer to the drain as the drain-source volt-

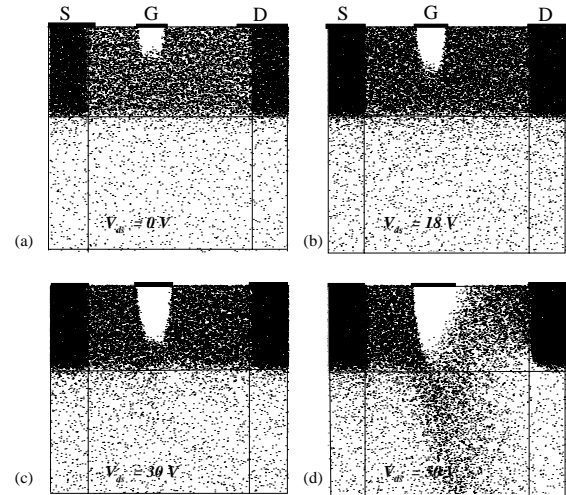


FIG. 5: Depletion layer profiles for different drain and gate biases for GaN MESFET at room temperature.

age increases. Note also that the transition between the gate depletion region and the charge neutral bulk is far from sharp on the drain side. At a sufficiently negative gate potential the depletion layer punches through to the high-resistivity buffer layer, and the source and drain electrodes are connected only by leakage paths within the buffer layer and substrate (see figure 5d).

An important factor in the high frequency performance of the MESFET is the time taken for electrons to traverse the region of the device beneath the gate, and the performance is enhanced by a high average electron velocity through that region.

The spatial distribution of hot electrons throughout the device for each valley at $V_{gs} = -1 \text{ V}$ and $V_{ds} = 50 \text{ V}$ for room temperature operation is shown in figure 6. Electrons are seen to exist in the upper valleys only to the right of the high field region, which exists on the drain side of the gate, because it is only there that the electrons have attained enough energy to be scattered into the satellite conduction valleys. Also note there is an injection of electrons from the channel into the buffer layer; a process which is eventually opposed by the electric field created by the resulting negative space charge in the buffer layer. Figure 6 also shows that the distribution of electrons occupying the upper valleys extends a significant way towards the drain region where the electric field is much lower. This is a result of the finite time that it takes for phonon scattering to return the electrons to the Γ -valley. Figure 7 shows the valley electron occupancies throughout the device. It can be seen that significant electron transfer to the upper valleys only begins to occur under the gate. Approximately 20% of the electrons occupy the higher valleys (mainly U and M valleys) in the vicinity of the gate which is similar to the valley occupancy ratio in the active layer of the $n^+ - n - n^+$ diode.

Figure 8 shows various microscopic properties of the device when the source-drain bias is 50 V and the gate voltage is -1 V ; specifically the longitudinal electric field, the Γ -valley band profile, the electron kinetic energy, the average drift velocity and the total electron density as a function

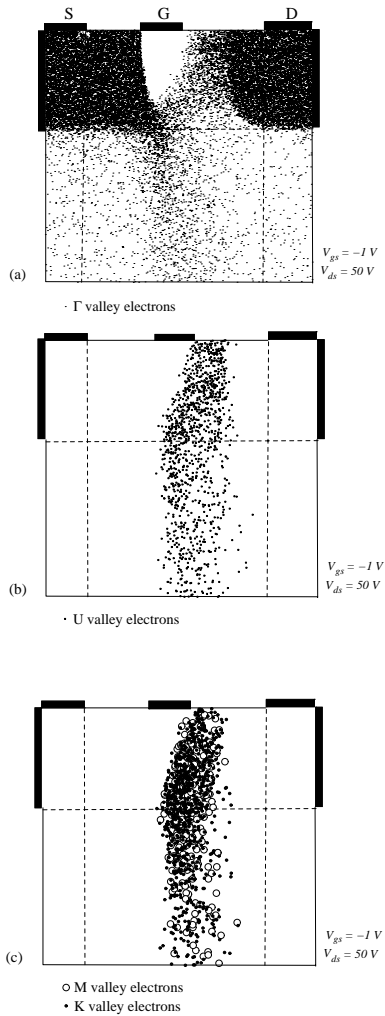


FIG. 6: The distribution of hot electrons at room temperature for $V_{gs} = -1$ V, $V_{ds} = 50$ V in central Γ valley and upper valleys.

of distance from the source. The longitudinal electric field plotted in figure 8a shows the high electric field in the region under the gate, which has been referred to earlier. Related to this is the Γ -valley band profile throughout the device in figure 8b. Note almost all the drain-source potential is dropped within the gate-drain region, leaving a flat potential profile near the source and drain. As electrons move towards the drain, they lose potential energy and gain sufficient kinetic energy to transfer to the upper conduction valleys where their drift velocity is reduced. The variations of average electron kinetic energy and average drift velocity throughout the simulated device are shown in figures 8c and 8d, respectively. The average electron velocity reaches about 2.1×10^5 ms^{-1} and then declines towards the drain. The step decrease in the average kinetic energy on the drain side of the gate is due to the transfer of electrons to the upper valleys. The electron density through the device is shown in figure 8e. The gate depletion region is clearly seen where the electron density is several orders of magnitude lower than it is near the source and drain.

The drain current is obtained by counting the net charge flow through the drain contact. Figures 9a and 9b show the

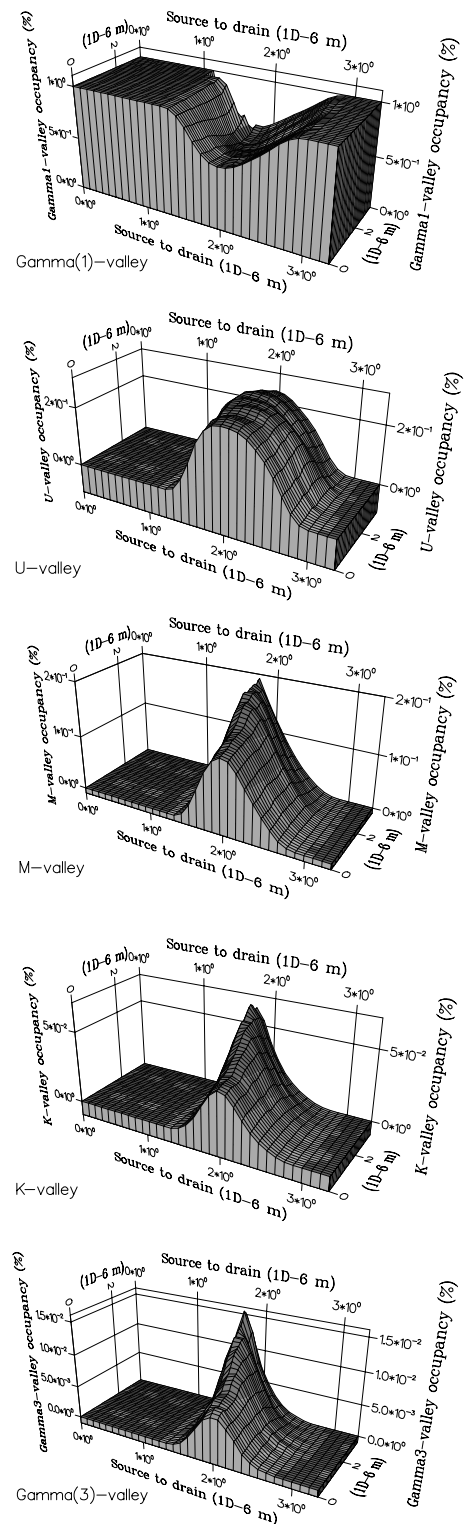


FIG. 7: The valley occupation ratios for the central Γ_1 -valley and upper valleys when the source-drain bias is 50 V and the gate voltage is -1 V at $T = 300$ K.

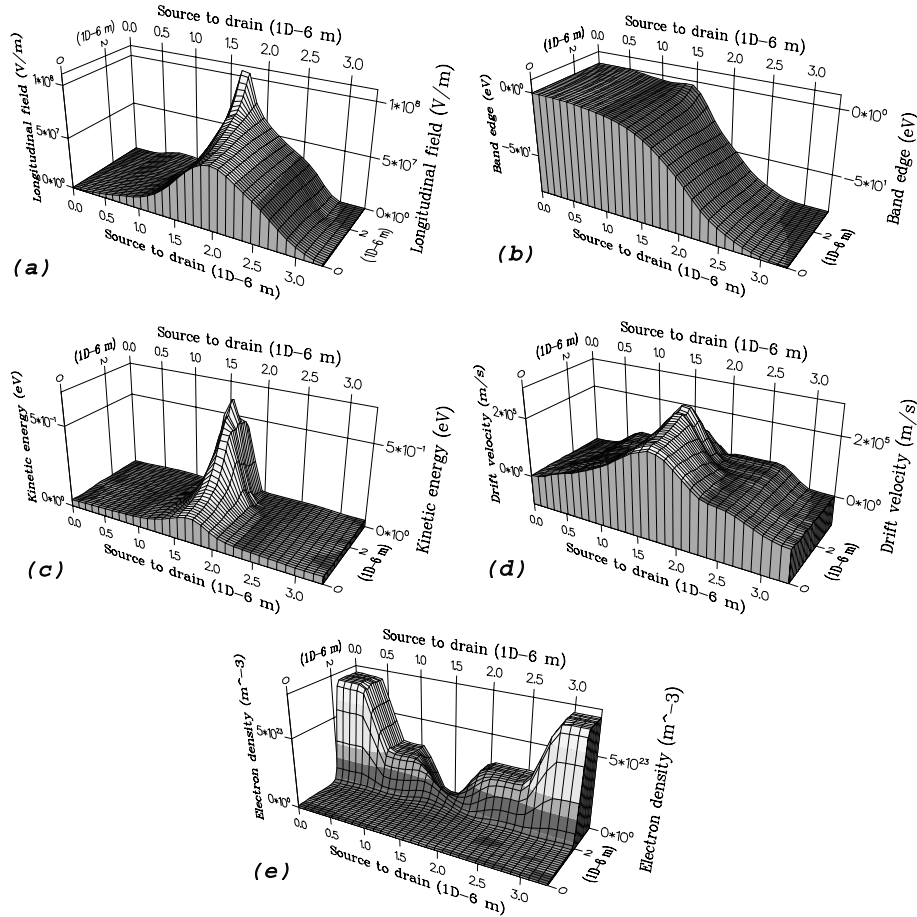


FIG. 8: Three dimensional distribution of electron data recorded through the simulation of the GaN MESFET when the source-drain bias is 50 V and the gate voltage is -1 V at room temperature. This figure shows: (a) Longitudinal electric field, (b) Γ -valley conduction band profile, (c) Average kinetic energy, (d) Drift velocity and (e) Electron density.

calculated drain current versus drain-source voltage at different gate biases for temperatures of 300 K and 420 K. Figure 9c shows the experimental results for the same device obtained by Trassaert *et al.*[17] at 300 K and a further presentation of the simulation results to facilitate comparison. The simulated characteristics at 300 K show good saturation behaviour with a knee voltage around 20-30 V and a saturation drain current of about 2200 mA mm^{-1} for $V_{gs} = 0$ V. The high drain current density is encouraging for the use of GaN for high-power applications.

Figure 9c shows the the simulated I - V characteristics is in fair agreement to the experimental measurements.

From figure 9a it is clear that the device is not completely pinched-off even at large negative gate bias ($V_{gs} = -15$ V) which is due to strong electron injection into the buffer layer at high electric fields. An increasing fraction of the drain current flows through the buffer as the drain voltage increases. At $V_{ds} = 80$ V essentially the whole drain current flows entirely through the buffer. To obtain some idea of the effect of high temperature on GaN MESFETs, simulations were carried out at $T = 420$ K, keeping the other device parameters unchanged. The I - V curves obtained are shown in figure 5.7b. Comparing the I - V curves at $T = 300$ and 420 K, it can be seen that the drain current is somewhat lower at the higher

temperature, due to increased phonon scattering, but the effect is not major. The transconductance of the MESFET is given by

$$g_m = \left. \frac{\Delta I_d}{\Delta V_g} \right|_{V_d} \quad (2)$$

and is calculated from figure 9a to be about 140 mS mm^{-1} at 18 V drain bias and -1 V gate voltage for room temperature. When the drain bias is increased to 50 V at the same gate voltage, the transconductance increases approximately to 200 mS mm^{-1} . In comparison, good GaAs MESFETs without a gate recess have a transconductance around 110 mS mm^{-1} [18-19]. The higher value of transconductance in simulated GaN MESFET is related to a higher drain current.

Conclusions

The operation of a GaN MESFET using a five valley model has been simulated by the Monte Carlo model. It is investigated that including higher valleys in the simulated device is important because more than %20 of the electrons occupy the higher valleys (mainly U and M valley) which

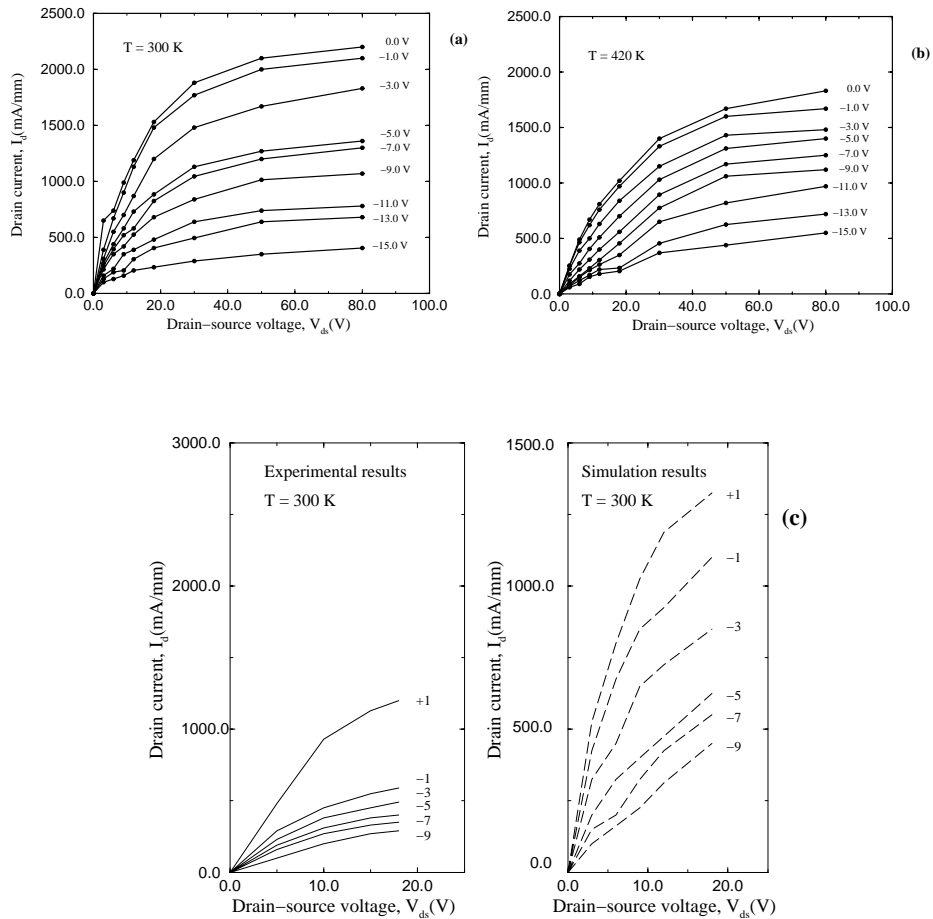


FIG. 9: (a) The simulated drain current versus drain voltage at $T = 300$ K, (b) The simulated drain current versus drain voltage at $T = 420$ K and (c) Comparison of the experimental I - V characteristics for the same device at $T = 300$ K with the simulated device.

will produce a serious reduction in the drain current and consequently the output power of GaN MESFET. Also the high output drain currents of the simulated device shows GaN is a good candidate for high-power and high-temperature applications.

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