Specification and Design of an Ethernet Interface Soft IP

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Abstract *The **IP** (Intellectual Property) for Ethernet Interface is a hardware module designed to execute the MAC (media access control) service on the Ethernet standard. The goal of this IP module is to provide an easy way to develop new devices with connection to an Ethernet LAN (Local Area Network). The standard protocols used make this IP module reusable for different designs with an interface to Ethernet LANs. The Ethernet Interface IP is described and simulated in VHDL*

Keywords: *Ethernet interface, local area network, design with VHDL, IP, VLSI design*

1 Introduction

The computing scene today is dominated by the interconnection of different devices, in a distributed architecture extending the communication possibilities. The explosion of the Internet, the exponential use of the e-mail, and new services like videoconference, video on demand, etc, contribute for an increasing need for connectivity. A new set of low-end, low-cost devices, named internet appliances, will reach the market in the niche of home and office automation, all of them enabled with some sort of low-cost network connectivity, using wires and 10baseT connectors. Conventional ethernet speeds will suffice for those devices, while GigabitEthernet and 100baseT will be applied solely for computer interconnections and fast data links.

The concept of computer networks is extremely large. However, it is possible to differentiate generically the computer networks in accordance with its area of coverage. Thus, Local Area Networks (LAN) are generally confined to a building or even a campus, Metropolitan Area Networks (MAN) are restricted to campus, blocks or to urban perimeters of great cities and Wide Area Networks (WAN) connecting cities, countries and continents.

Currently two technologies are dominant in the LAN environment: the Ethernet standardized by the IEEE as 802.3, and the Token ring, represented by norm IEEE802.5. The Ethernet technology is based on a shared environment, using protocol CSMA/CD for determination of physical network access. The standard IEEE 802.3 defines three physical media, baseband or wideband coaxial cables, as well as twisted wires. The use of the twisted wire cables, called 10BaseT, has become popular. It can connect a large number of workstations using hubs or switches, physically connected as a star network, but logically connected as a bus. The Token Ring technology uses a special frame called “Token”, which determines which workstation has the right to access the wire that is physically and logically organized as a ring. However, the Ethernet is the most used due to its easiness of implementation, tolerance to errors and its production in large scale. An isolated computer, device or resource which lacks this interface does not satisfy current com-

munication needs. It is then compelling that each device to be connected to an Ethernet Local Area Network have an Ethernet Interface.

2 The CSMA/CD Access Method

The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) media access method is the means by which two or more station/devices share a common transmission medium. In transmission mode, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then it sends the intended message in a bit-serial form. If, after initiating a transmission, the message collides with one from another station, then each transmitting station intentionally sends a few additional bytes to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (back off) before attempting to start transmission again.

The CSMA/CD media access method is standardized by IEEE 802.3 [1][2] and it belongs to the MAC (media access service) sublayer. The MAC sublayer and the Logic Link Control sublayer together encompass the functionality intended for the Data Link layer as defined in the OSI Model. The physical layer and the Data Link layer standardized by IEEE 802.3 are intended to correspond closely to the lowest layers of the ISO Model for Open Systems Interconnection (see figure 1) [3].

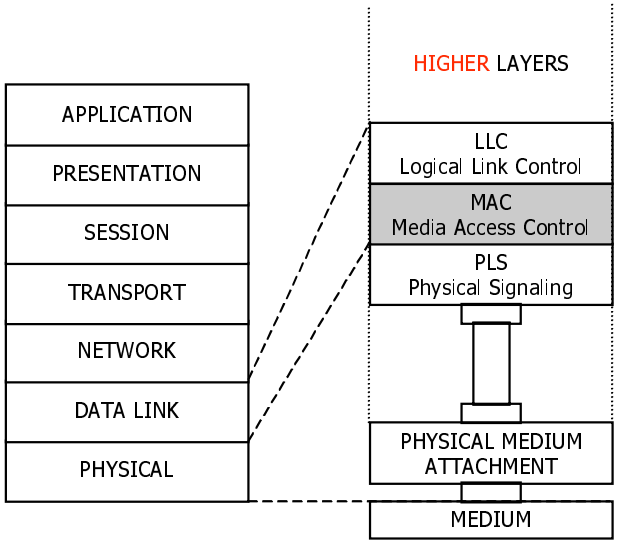

Figure 1: IEEE LAN Standard relationship to OSI Reference Model.

The CSMA/CD media access method is the same method used in the Ethernet standard. However, there is a difference between the Ethernet standard and the IEEE 802.3 in the structure of their frames. In the Ethernet frame there is a field called type and in the standard IEEE 802.3 the size of the frame is given in this field. But this difference does not cause problems to implement the IEEE 802.3 standard CSMA/CD method in an Ethernet Interface.

2.1 Ethernet Frame Structure

Figure 2 shows the seven fields of a frame: the preamble, Start Frame Delimiter (SFD), the addresses of the frame's source and destination, a type field, the data to be transmitted and the Frame Check Sequence (FCS) containing a cyclic redundancy check value to detect errors in received frames. All these fields are fixed size except the Data, which may contain an integer number of octets.

The preamble field is a 7-octet(or 7-byte) field that is used to allow the PLS circuitry to reach its steady-state synchronization with the received frame timing. The start frame delimiter field is the sequence 10101011. It immediately follows the preamble pattern and indicates the start of a frame.

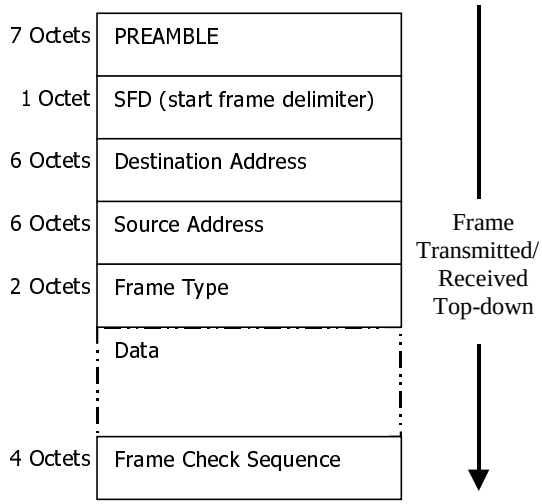

Figure 2: Ethernet Frame Format

The frame check sequence field contains a 4-octet (32-bit) cyclic redundancy check (CRC) value. This value is computed as a function of the contents of source address, destination address, type and data.

An invalid Ethernet frame shall be defined as one that meets at least one of the following conditions:

(i) the frame does not have an integral number of octets in length;
(ii) the bits of an incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received[4];
(iii) the frame length is shorter than the minimum frame size.

2.2 CSMA/CD Access Method Functional Capabilities

The following summary shows a quick reference of the functional capabilities of CSMA/CD MAC sublayer.

In frame transmission:

- accept data from the LLC sublayer and construct a frame;
- present a bit-serial data stream to the physical layer for transmission on the medium.

In frame reception:

- receive a bit-serial data stream from the physical layer
- present to the LLC sublayer frames
- defer transmission of a bit-serial stream whenever the physical medium is busy
- append proper FCS value to outgoing frames and verify full octet boundary alignment
- checks incoming frames for transmission errors by way of FCS and verifies octet boundary alignment
- delay transmission of frame bit stream for specified interframe gap period
- halt transmission when collision is detected
- schedule retransmission after a collision until a specified retry limit is reached
- enforce collision to ensure propagation throughout network by sending jam message
- discard received transmission that are less than a minimum length
- append preamble, start frame delimiter and FCS to all outgoing frames
- remove preamble, start frame delimiter and FCS to all incoming frames

3 The Ethernet Interface IP

The Ethernet Interface IP is a hardware module design to implement all CSMA/CD functional capabilities. However, the physical layer must be handled by an universal transceiver. So, the physical layer interface specification was designed using the LXT901A/907A Universal Transceiver chip of Level One[5].

The LLC interface provides an easy way to transform data between Ethernet Interface and other devices. These devices can implement the LLC sublayer or can use the Ethernet Interface to enable their communication using Ethernet standard. Figure 3 shows the I/O of the Ethernet Interface IP.

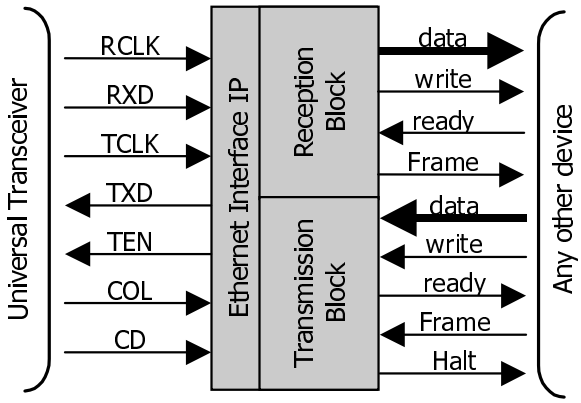

Figure 3: The Interfaces of Ethernet Interface

The RCLK signal is a 10MHz clock used to synchronize the input bit-serial stream on the RXD. In the same way, the TCLK is a clock used to synchronize de output bit-serial stream on the TXD, but the TEN(Transmit Enable) must be used to enable the transceiver to transmit the outgoing bit-serial stream. The COL (collision detect) pin indicates when the collision occurs and the CD (carrier detect) indicates when the medium is busy.

The Ethernet Interface was divided in two independent blocks: transmission block and reception block. These blocks work concurrently, but the CD signal does not allow simultaneous transmission and reception.

To allow all CSMA/CD functional capabilities, two algorithms were specified. The first one, shown in figure 4, implements the transmission tasks in the transmission block. The second one, shown in figure 5, performs the reception task in the reception block.

In the reception block, data is a 16-bit line output where the reception block will enable the frame data (destination address, source address, data) incoming from LAN. When a new word is ready on 16-bit line the write signal warns. If the frame line is equal to 1 then the data contains frame data. In other way, if the frame line is equal to 0 then data contains a validation word.

At the end of frame reception, the reception block will check to validate the received frame. After a valid frame reception, the reception block will send a validation word that is the received frame length (an integer number of octets). Under this condition, always the two most significant bit of the data line are set to 1. Con-

versely, after an invalid frame reception, the reception block will send an invalidation word that contains the two most significant bits set to 0.

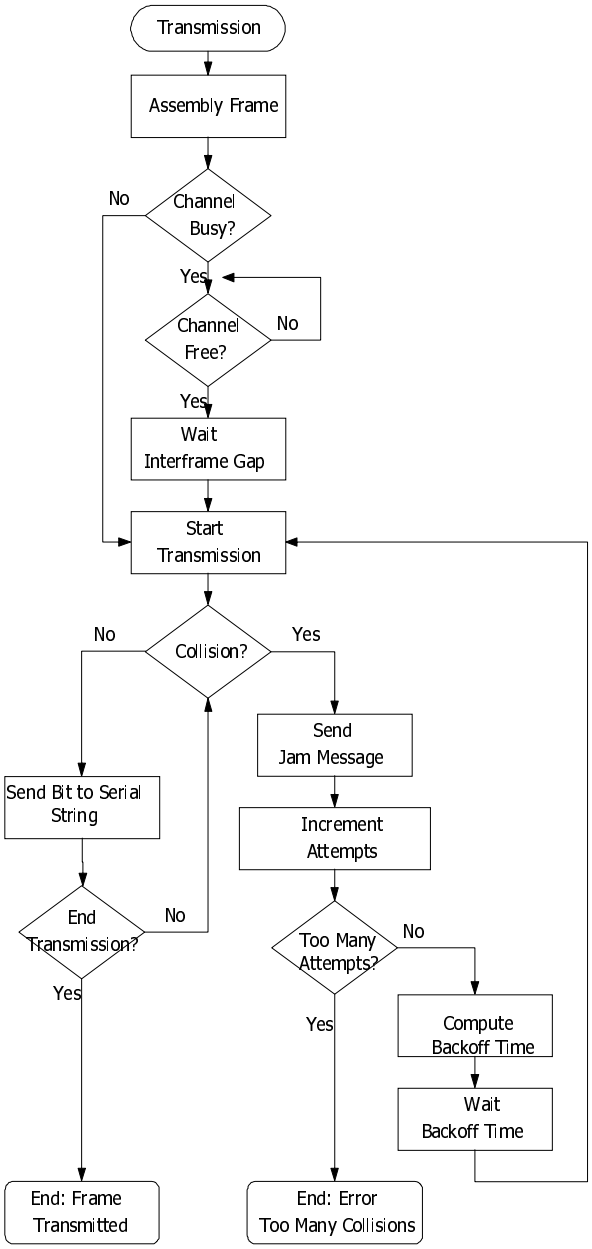

Figure 4: Transmission Algorithm

The ready input line indicates when the 16-bit line is ready for new data. If a new data is coming and the data line is not ready (ready line equals to 1), the reception block will discard the entire incoming frame. Figure 6 shows the reception block interface protocol.

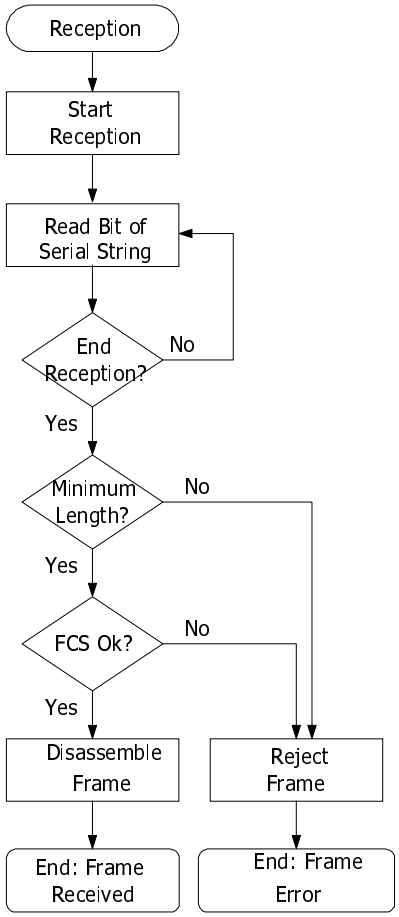

Figure 5: Reception Algorithm

In the transmission block, data is a 16-bit line input where the devices connected to the Ethernet Interface will enable the frame data (destination address, source address, data) intended to the LAN.

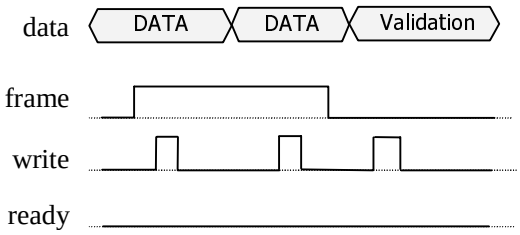

Figure 6: Reception Block Interface Protocol

The reception block works in a similar way, when a new word is ready in the 16-bit line the write signal warns. If the frame line is equal to 1 then the data contains frame data. If not, frame line equals to 0, then data contains the output frame length in number of octets.

The device intended to send data to LAN must send ahead to the transmission block the validation word (length of data frame and two most significant bits set to one). The transmission block will use the length to con-

trol the output bit-serial stream.

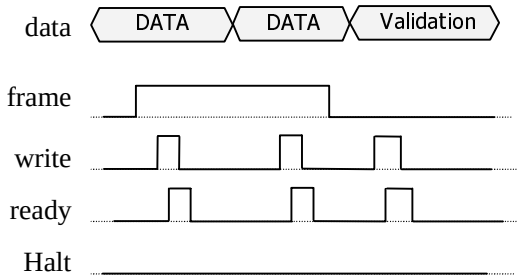

Figure 7: Transmission Block Interface Protocol

The ready signal indicates when the 16-bit line is ready for a new data (ready equal to 0). The ready will remain equal to 1 until the last data sent by a device is processed. When the ready becomes 0 the new word must be put in data line.

If there is a contention in the transmission (probably a collision), the signal Halt will indicate to the device that the outgoing frame must be retransmitted. Then, the device must send the data from the beginning (including the length of data frame). Figure 7 shows the transmission block interface protocol.

4 Results

The Ethernet Interface was described in VHDL. In order to validate, the VHDL description was simulated using the ALTERA MAXPLUS II tools. The transmission simulation results are shown in figure 8 and figure 9. Figures 10 and 11 show the reception simulation results.

These simulations had a 25ns clock period. The frequency may change as a result of choices in the technology and type of implementation used.

The Ethernet Interface input signals from the universal transceiver and the any other device, showed in figure 3, was described using the waveform editor from MAXPLUSII. The timing of these signal conform to the transceivers and the protocol specified to communicate to other devices.

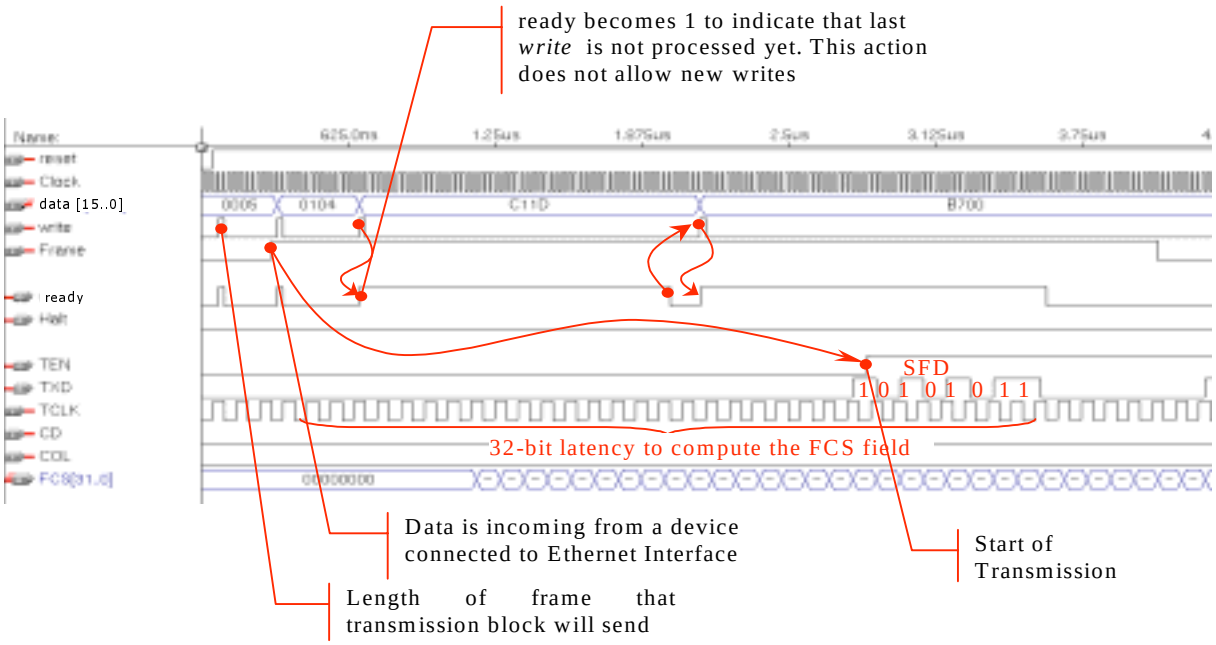

Figure 8 : The start of a frame transmission

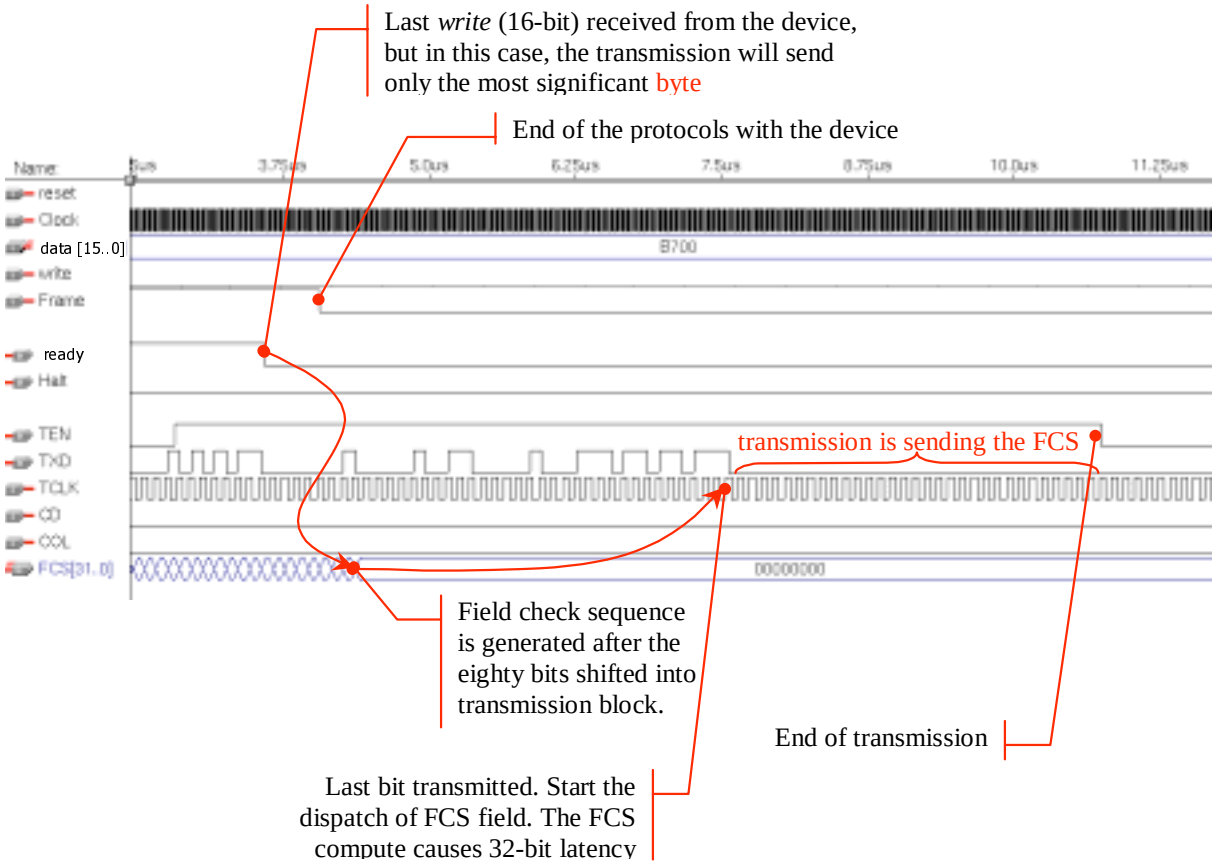

Figure 9: The end of a frame transmission

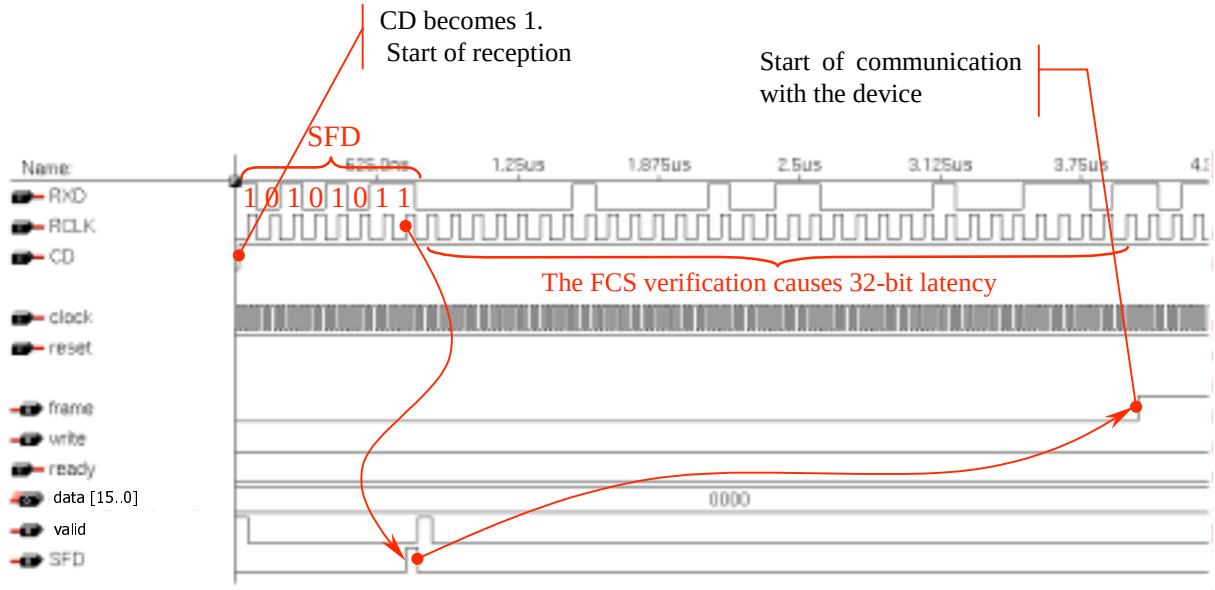

Figure 10: The start of a frame reception

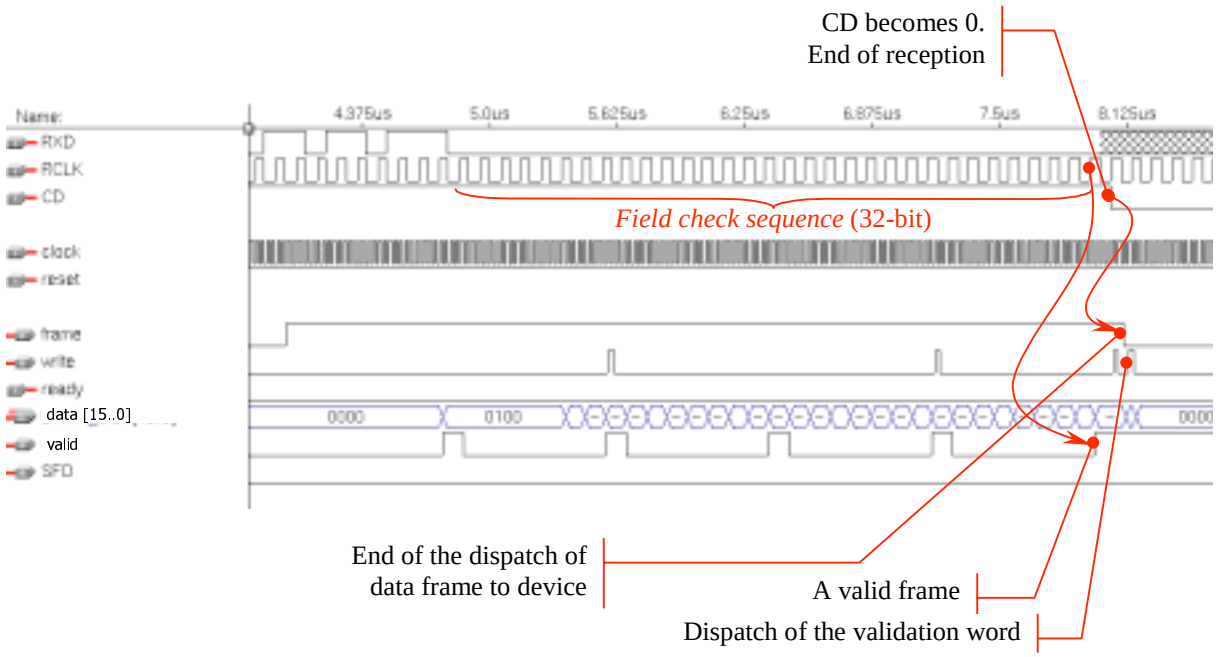

Figure 11: The end of a frame reception

5 Example of an application

The first application of this IP is in the design of a LAN Bridge ASIC, the LAWAI [5] chip under development at the UFRGS Computer Science Institute.

The LAWAI chip has two subsystems: one that performs the LAN interface and the other that carries through the WAN interface. The chip is divided into 4 main blocks: the LAN controller interface (responsible for the reception and transmission of the Ethernet frames through the transceiver), the WAN controller interface (responsible for the reception and transmission of the frames to the network WAN), the frame stream controller IP, responsible for the writing and reading of the frames in the memory and the reception and transmission priorities management, and the controller of SDRAM memory.

This circuit is placed in an intermediate market niche, between the networks of great corporations that need routers and the small networks that need only switches and hubs. Even though significant results were obtained in functional partition, specification, and simulation, many other developments are still needed in the future to develop a hardware IP. The Bridge ASIC developed is transparent, or in other words, it indiscriminately passes the information from one side to another side of the network. The algorithms of self-learning and spanning tree [1] must be implemented in this chip.

6 Conclusions

This work presented an Ethernet Interface IP designed and simulated using VHDL. It is a software IP implementing the standard, and it can be used as a module in the design of any device that needs an Ethernet LAN communication interface. The use of IP modules is important to reduce the design cycle and design costs of a new product.

The application of reusable IP modules is increasing due to the increasing demand for embedded systems. Ethernet Interface IP has a great potential for a vast range of applications that require Internet connectivity, be it in appliances, peripherals and devices that will be made Internet-ready in the future.

References

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