A JL-SDR-IMPATT Device with Improved Efficiency

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Abstract—**An attempt has been made to present a new device which will function as a highly efficient SDR (Single Drift Region) P+-N-N+ IMPATT diode utilizing the advantages of a junctionless field effect transistor. The basic idea is to convert a uniform N+ region into a (P+–N–N+) structure without any requirement of physical doping. As the present device works on the principle of a junctionless channel, variability and short channel effects are significantly reduced as compared to the conventional TFET though the requirement of an extra gate increases a few fabrication steps. Further, efficiency more than conventional SDR IMPATT diode is achievable without any physical doping.**

Index Terms—ControlGate, efficiency, electric field, IMPATT, P-gate, SDR.

I. INTRODUCTION

The IMPATT (IMPact-Avalanche-Transit Time) diode is a popular transit time device which gains its reputation in microwave (3-30 GHz) and millimeter wave (30-300 GHz) digital and analog communication systems as well as in radar for civilian purposes and for defense systems in missiles. In order to produce negative resistance at microwave frequencies, these diodes utilize impact ionization and transit time properties of semiconductor structures. Impact ionization is a process of formation of additional holes and electrons by knocking them out of the crystal structure due to high electrons and holes velocity. In IMPATT devices, negative resistances arise from two delays (avalanche delay-caused by finite build-up time of avalanche current, transit time delay- caused by the finite time taken by the carriers to cross the drift region) which cause the current to lag behind voltage [1]. These two delays add up to 180^0 phase lag at a particular frequency and so the diode resistance is negative corresponding to that frequency.

On the other hand, it is observed that the characteristics of a nano-scale Metal Oxide Semiconductor Field Effect Transistors (MOSFET) have deteriorated owing to continual down scaling in size. Due to continual reduction in the dimensions of the MOS devices, various short channel effects (SCEs) such as Drain Induced Barrier Lowering(DIBL), gate tunneling, punch through, surface scattering etc are very much predominant along with several severe fabrication issues (especially in the sub-20nm channel region). So continuous efforts have been made in the recent years to improve the SCE immunity by using single as well as dual material double gate SOI/SON MOSFET structures [2-5].

However, these severe issues especially that of fabrications have been reduced by junctionless tunnel Field effect Transistor (absence of physical p-n junction in the source or drain side) where only a uniformly doped channel has been present [6-11].This structure produces excellent immunity to SCEs (Short Channel Effects) and double-gate or multi-gate devices offer better scalability options. Besides, this device is simpler to fabricate and has less variability and better electrical properties than MOSFET. So, these attractive advantages of the junctionless TFETs encourage us to use this kind of devices as junctionless SDR IMPATT device.

At different millimeter-wave window frequencies, Si and GaAs IMPATTs are already established as efficient and powerful sources [12-14]. For generation of RF power at THz frequencies, the potentiality of wide band-gap materials (GaN,SiC) has been reported in the recent years. Though different semiconductor materials like GaAs, InP, GaN have been used for IMPATT development to achieve higher efficiency, power output and frequency range, silicon still remains the most reliable material for millimeter-wave IMPATTs owing to its advanced technology and stability. The device efficiency of a silicon SDR (p+-n-n+) IMPATT diode at Ka-band is found to be 7.84%-8.98%. The maximum efficiency observed for 4H-SiC SDR IMPATT diodes is 23.28% (for Ka band) [15-17].Since this efficiency is quite low, continuous efforts have been made in the recent years to increase the efficiency.

In this paper, an attempt has been made to present a new device which will function as a highly efficient SDR (Single Drift Region) P+-N-N+ IMPATT diode utilizing the concept of a junctionless field effect transistor. The basic idea is to convert a uniform N+ region into a (P+–N–N+) structure without any requirement of physical doping. Since this device is based on the principle of a junctionless channel, variability and short channel effects immunity improves as compared to the conventional TFET though the requirement of an extra gate increases a few fabrication steps. Besides without any physical doping greater efficiency can be achieved than that of a normal SDR IMPATT diode.

II. DEVICE DESCRIPTION

The proposed device structure is a lateral n+-type JLFET which uses two isolated gates (Control Gate and P-gate) of two different metal work functions, to make the layer beneath the gates n-type and p+-type. We have chosen the metal work function as 4.27 eV and 5.93eV for the CG and PG electrode, to make the layer beneath the CG and the PG electrode n-type and p+-type respectively [18-19]. As soon as the contact is made between metal oxide and the N+ semiconductor, the electrons will flow from the semiconductor to the metal and thus Fermi level goes down and in equilibrium this level is aligned with the Fermi level of the metal. For higher metal work function, more and more electron flow from the semiconductor to the metal and the Fermi level goes down more towards the valence band. In this way, a N+ region can be converted to N and P+ region depending on the metal work function .The CG and PG are both kept at zero bias.
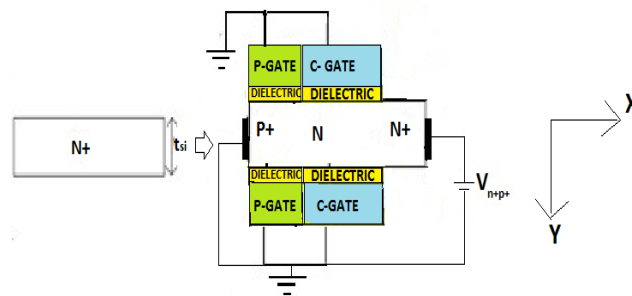
Fig.1.   The device structure indicating the N+ ,N and P+ regions along with the Control gate and P gate where two different metals(indicated by blue and green) and oxide layers(indicated by yellow).
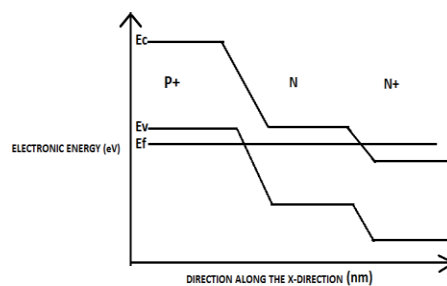

Fig.2.   The approximate energy band diagram for the N+, N and P+ regions

III.   ANALYTICAL MODEL OF ELECTRIC FIELD AND EFFICIENCY

Considering n+ degenerate type semiconductor bar, the position of the Fermi level for this degenerate semiconductor can be written as [20]

$$E_{Fn+} = E_c + kT[ln(\frac{n_{n+}}{N_c}) + 2^{-\frac{3}{2}}(\frac{n_{n+}}{N_c})] \tag{1}$$

where N_c is the carrier density in the conduction band, k is the Boltzmann's constant, T is the temperature in Kelvin, n_{n+} is the carrier concentration in the n+ bar and E_c is the conduction band energy

The position of the Fermi level for a n- type region can be written as

$$E_{Fn-} = E_c + kT[ln(\frac{n_{n-}}{N_c})] \tag{2}$$

where n_{n-} -the carrier concentration in the n region

Solving equations (1) and (2) we get,

$$E_{Fn-} = E_{Fn+} + kT[ln(\frac{n_{n-}}{n_{n+}}) - 2^{-\frac{3}{2}}(\frac{n_{n+}}{N_c})] \tag{3}$$

Again, the position of the Fermi level for a p+ degenerate type region can be written as

$$E_{Fp+} = E_v - kT[ln(\frac{p_{p+}}{N_v}) + 2^{-\frac{3}{2}}(\frac{p_{p+}}{N_v})] \tag{4}$$

where p_{p+} is the concentration of the p+ region and N_v is the carrier density in the valence band

Now, solving equations (1) and (4) we get

$$E_{Fp+} = E_{Fn+} - E_g - kT[ln(\frac{p_{p+}n_{n+}}{N_c N_v}) - 2^{-\frac{3}{2}}(\frac{n_{n+}}{N_c} + \frac{p_{p+}}{N_v})] \tag{5}$$

The metal work functions for the Control gate and the P-gate can be expressed as

$$\phi_{MC} = \phi_{sn+} + (\frac{E_{Fn+} - E_{Fn-}}{q}) \tag{6}$$

$$\phi_{MP} = \phi_{sn+} + (\frac{E_{Fn+} - E_{Fp+}}{q}) \tag{7}$$

where ϕ_{MC} ϕ_{MP} -the metal work functions for the Control Gate and the P-gate and ϕ_{sn+} -the semiconductor work function

Solving the above equations we get,

$$\phi_{MC} = \phi_{MP} + (\frac{E_{Fp+} - E_{Fn-}}{q}) \tag{8}$$

The conditions for converting the N+ region to intrinsic-type, n-type and p+-regions
are $\Delta E_{min} = \frac{E_g}{2} - 3kT, \Delta E < \Delta E_{min}, E_g - 6kT > \Delta E > \Delta E_{min}$ and $\Delta E > E_g - 6kT$

Now, from the 2D-Poisson's equation, the electrostatic potential profile can be written as

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_D}{\varepsilon_{si}} \tag{9}$$

where N_D is the donor concentration in the n region of the device, q is the electronic charge and ε_{si} is the silicon substrate permittivity.

An approximate solution of the 2D potential distribution can be proposed assuming a parabolic potential as suggested by Young [21]

$$\psi(x, y) = \psi_s(x) + a_1(x)y + a_2(x)y^2 \tag{10}$$

where $\psi_s(x)$ -the surface potential which varies along the channel a_1, a_2 are functions of x.Now, introduction of symmetric conditions with respect to $\frac{t_{si}}{2}$ [22] leads to

$$\psi(x, y) = \psi_s(x) + a_1(x)y - \frac{a_1(x)y^2}{t_{si}} \tag{11}$$

where t_{si} -the substrate thickness

With the introduction of boundary conditions at the surface i.e. $\frac{\partial \psi(x, y)}{\partial y}\Big|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(\psi_s(x) - V_{gp+^i})}{t_{ox}}$,we then derived an expression for $a_1(x)$

$$\frac{\partial \psi(x, y)}{\partial y}\Big|_{y=0} = a_1(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(\psi_s(x) - V_{gp+^i})}{t_{ox}} \tag{12}$$

where $V_{gp+^i} = V_{gp+} - \phi_{MS}$ and t_{ox} -the oxide thickness

Substituting the value of $a_1(x)$ from equation (12) to (11) we get,

$$\psi(x, y) = \psi_s(x)[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{y}{t_{ox}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{y^2}{t_{ox}t_{si}}] + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{gp+^i}}{t_{ox}}[\frac{y}{t_{si}} - 1] \tag{13}$$

Now, substituting the above expression of $\psi(x, y)$ in (9), a new differential equation in terms of the surface potential is obtained as

$$\frac{\partial^2 \psi_s}{\partial x^2} - \frac{2\varepsilon_{ox}\psi_s(x)}{\varepsilon_{si}t_{ox}t_{si}} + \frac{2\varepsilon_{ox}V_{gp+^i}}{\varepsilon_{si}t_{ox}t_{si}} = \frac{qN_D}{\varepsilon_{si}} \tag{14}$$

Let $M = \dfrac{2\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}}$, $P = \dfrac{qN_D}{\varepsilon_{si}} - MV_{gp+^i}$

Therefore, the equation (14) simplifies to

$$\frac{\partial^2 \psi_s(x)}{\partial x^2} - M\psi_s(x) = P \tag{15}$$

Solving the differential equation of (7) we get

$$\psi_s(x) = Ae^{\delta x} + Be^{-\delta x} - \frac{P}{M} \tag{16}$$

where $\delta = \sqrt{M}$

Now, the boundary conditions-

$\psi_s(0,0) = \psi_s(0,t_{si}) = V_{bi}$, $\psi_s(L,0) = \psi_s(L,t_{si}) = V_{bi} + V_{n+p+}$ have been used to solve for the constants A and B

$$B = \frac{(V_{bi} + \dfrac{P}{M})e^{\delta L} - (V_{bi} + V_{n+p+} + \dfrac{P}{M})}{e^{\delta L} - e^{-\delta L}}$$

$$= (\frac{e^{\delta L}}{e^{\delta L} - e^{-\delta L}})[(V_{bi} + \frac{P}{M}) - (V_{bi} + V_{n+p+} + \frac{P}{M})e^{-\delta L}]$$

$$A = V_{bi} + \frac{P}{M} - B$$

where V_{n+p+} -the applied voltage across the p+ and n+ regions, V_{bi} - built-in potential

Now the expression of electric field can be obtained from differentiating the equation (16),

$$E_s(x) = \delta[Ae^{\delta x} - Be^{-\delta x}] \tag{17}$$

Now, if an ac voltage $v = V_{max}\sin wt$ is superimposed on applied dc voltage $V_r = V_{n+p+}$, the efficiency of the device is given by [23]

$$Efficiency(\eta) = \frac{2V_{max}}{\pi V_B} \tag{18}$$

where V_B is the breakdown voltage and is given by

$$V_B = x_A\xi_A + (W - x_A)\xi_D \tag{19}$$

where ξ_A , ξ_D are electric field in the avalanche and the drift region and x_A ,W are the avalanche width and depletion width where the electric field decays to zero.

The maximum ac voltage depends on swing in the electric field $\Delta\xi$ in the avalanche and drift region

$V_{max} = \Delta\xi W$

  Considering optimistic situation i.e. the voltage across the drift zone swings to zero thereby making the electric field zero at the maximum negative voltage of the ac voltage i.e. $\Delta\xi = \xi_D$ and the with the assumption that $\xi_A = 2\xi_D$,the efficiency can be modified as [23]

$$\eta = \frac{2}{\pi} \frac{1}{1 + \dfrac{x_A}{W}} \tag{20}$$

The avalanche width (x_A) can be derived from the equation (17) as

$$x_A = \frac{[\dfrac{E_{max}}{2} - \delta(A - B)]}{\delta^2(A + B)} \tag{21}$$

where $E_{max} = \delta(B - A)$

The depletion width on the other hand can also be derived from the equation (17) by setting the electric field as zero

$$W = \frac{ln(B \, / \, A)}{2\delta} \tag{22}$$

IV. RESULTS AND DISCUSSION

In this section, variations of electric field with the length along the drift region for different parameters, efficiency variations with carrier concentration, oxide permittivity and oxide thickness have been studied. Besides efficiency comparison has been made for the junctionless SDR IMPATT and conventional SDR IMPATT. Fig. 3 depicts the variation of the electric field with length along the drift region for two different biasing voltages of 0.5 V and 0.35 V (equivalent electric fields of more than $10 *10^7$ V/m), applied across the device i.e. between P+ and N+ regions. For an applied bias of 0.5 V and 0.35 V, the electric field is maximum at the P+-N junction as expected where avalanche breakdown occurs. It is to be noted that in silicon avalanche breakdown occurs at a field of $\sim 5 *10^7$ V/m- for carrier concentration of $10^{23}/m^3$ which we have used in our calculations[24]. It is thus established the occurrence of impact ionization at a biasing voltages of 0.5V and 0.35 V. The electric field decreases as we proceed along the drift region. Eventually it decreases to a value close to zero near the n+ region. Another significant observation is that the electric field decreases comparatively faster as the voltage, applied across the device is increased as with the increase of reverse bias, more and more electrons immobile acceptors are created in the N+ region and therefore the electric field decreases more rapidly at a higher reverse bias. It is depicted in Fig.4 that the electric field profile of the junctionless SDR IMPATT almost resembles that of a normal P+-N-N+ SDR IMPATT diode. In case of junctionless SDR, there may be some excess minority carrier concentration present in the very small gap (if present) between the region under P-gate and C-gate and also in the n-region due to imperfect conversion of the regions due to different metal work functions. So, the electric field decreases slightly in case of junctionless SDR compared to that of conventional SDR.
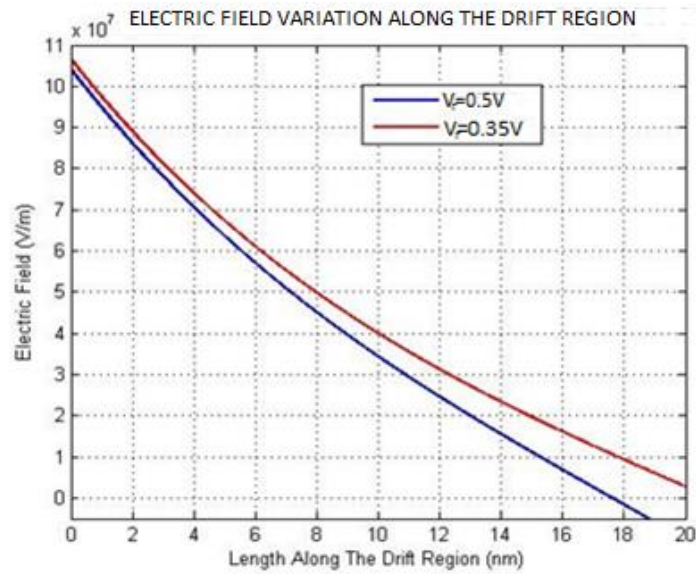
Fig.3. Electric field profile along the drift length L=20nm for two different applied voltages (V_r=0.5V, 0.35V).
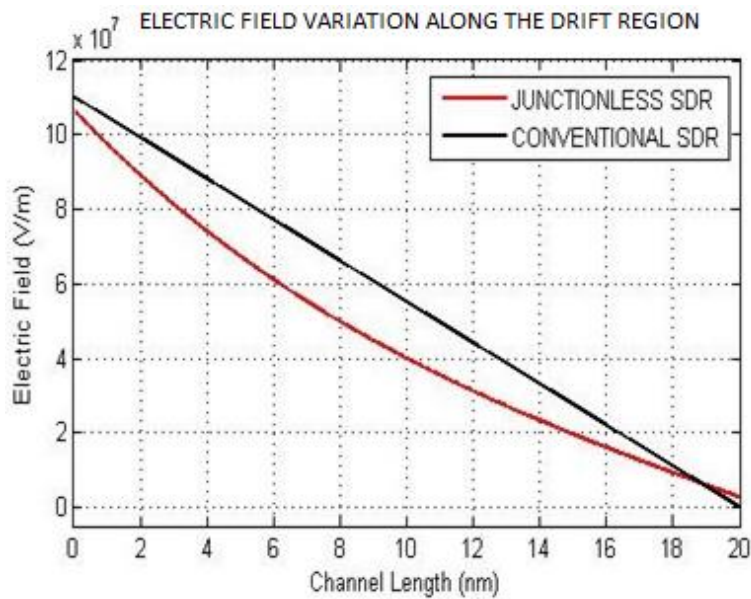

Fig.4. Electric field profile along drift length L=20nm for a junctionless SDR IMPATT and a conventional SDR IMPATT.

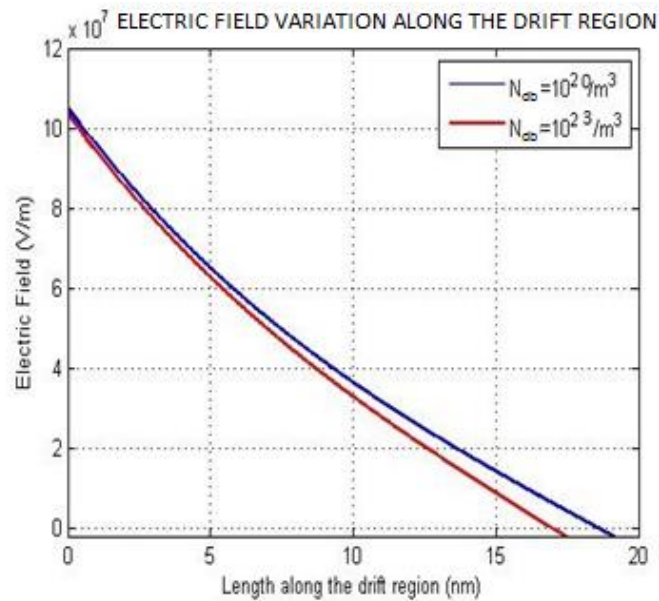Fig.5. Electric field profile along drift length L=20nm for two different carrier concentrations ($N_{db}=10^{20}$/m^3,10^{23}/m^3).

Fig. 5 represents the variation of the electric field with length along the drift region for two different n-region doping concentration .Again as earlier the electric field is maximum at the p+-n junction as expected where avalanche breakdown occurs and it decreases as we proceed along the drift region and eventually it decreases to a value close to zero at the end of the depletion width which is near the N+ region. But here it is observed that the electric field decreases to zero comparatively earlier with the increase of substrate doping concentration of the n-region as the small electric field between the n-N+ regions vanishes with the increase of doping concentration (n-region is tending to a N+ region).Thus effectively, the extension of the depletion width in the n-region will be reduced thereby lowering the electric field near the N+ region.

Fig. 6 represents the variation of the efficiency of this device with the oxide permittivity. The efficiency of the device increases rapidly with the increase of oxide permittivity. With the decrease of oxide thickness, the capacitance between the n-region and C-gate increases and so the immobile carrier concentration decreases in the n-region. Thus, the depletion width will increase in the n-region, thereby increasing the efficiency. By using high K dielectrics the efficiency of this device can be increased. Moreover high K-dielectric also provides high immunity to the leakage current when the device is in off-state.

Fig. 7 depicts the variation of the efficiency of this device with the oxide thickness. The efficiency of the device increases with the reduction of the gate oxide thickness. Besides the efficiency of the device increases for smaller silicon substrate thickness. Higher efficiency can be achieved for silicon substrate thickness of 12nm compared to that of 15nm silicon substrate thickness as shown in the figure. It should be noted that with the decrease of oxide or silicon thickness, there is modulation of

the immobile carrier concentration (decreases due to changeover of the N+ region to n-region) in the n-region and so the depletion width will increase as stated earlier and so the efficiency of the device will also increase.

Fig. 8 represents the variation of the efficiency of this device with the oxide thickness as shown earlier in the Fig. 7 but here the variations have been shown for two different applied voltages 0.5 V and 0.35V.As it can be clearly observed that higher efficiency can be achieved for 0.35V compared to the applied voltage of 0.5V .

Fig. 9 shows the variation of the efficiency of a junctionless SDR IMPATT and a normal SDR IMPATT with the substrate carrier concentration. It can be observed that the efficiency of the proposed device is comparatively higher for the junctionless SDR IMPATT than that of a normal SDR IMPATT thereby making this junctionless device more attractive. It should be noted that the maximum electric field is less in case of junctionless SDR IMPATT due to the reasons already mentioned earlier and so the avalanche width being dependent on maximum electric field will be less (equation 21) thereby making the efficiency of a junctionless SDR IMPATT greater than that of a conventional SDR IMPATT.
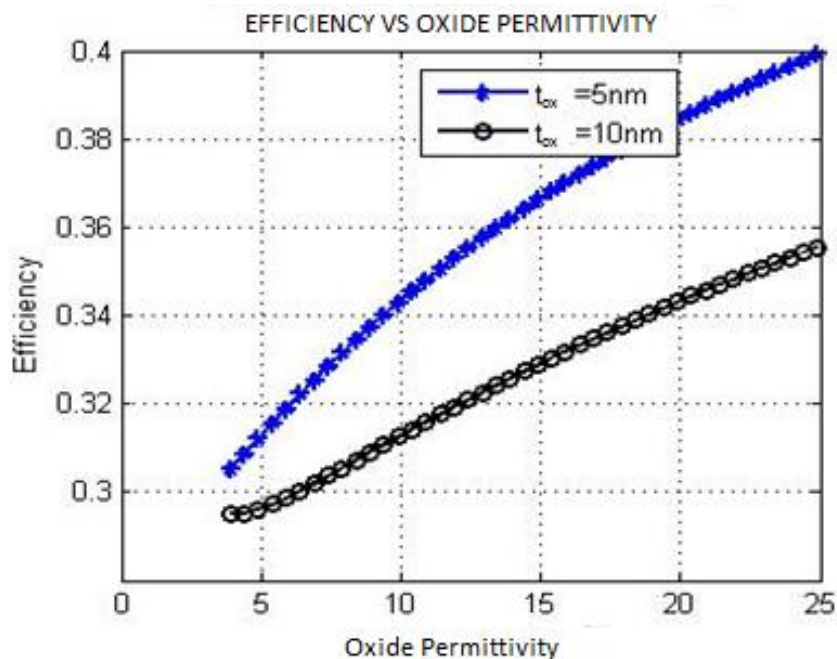

Fig.6. Variation of efficiency of junctionless SDR IMPATT device with the oxide permittivity for two different oxide thickness (t_{ox}= 5, 10 nm).
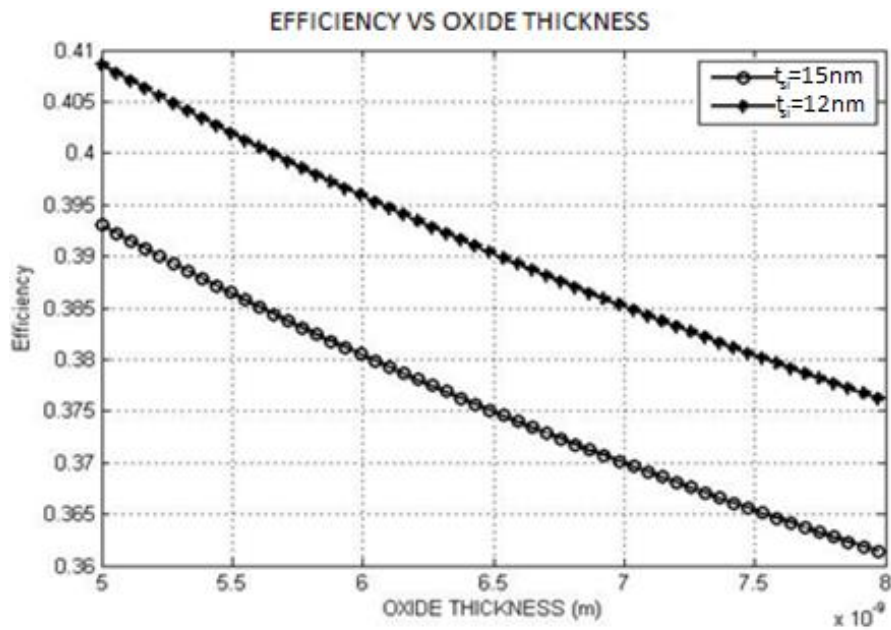
Fig.7. Variation of efficiency of proposed junctionless SDR IMPATT device with the oxide thickness for two different silicon body thickness (t_{si}=12, 15 nm).

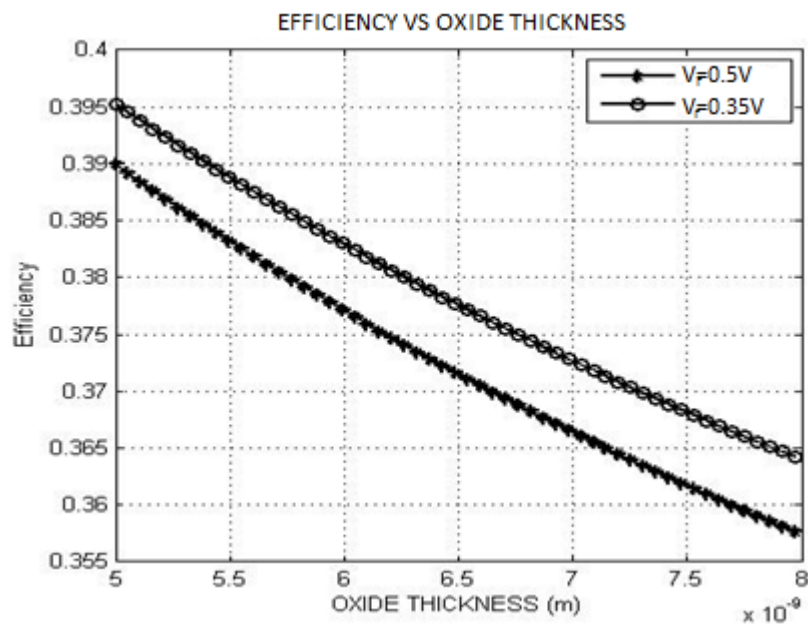Fig.8. Variation of efficiency of junctionless SDR IMPATT device with oxide thickness for two different applied voltages (Vr=0.5V, 0.35V).
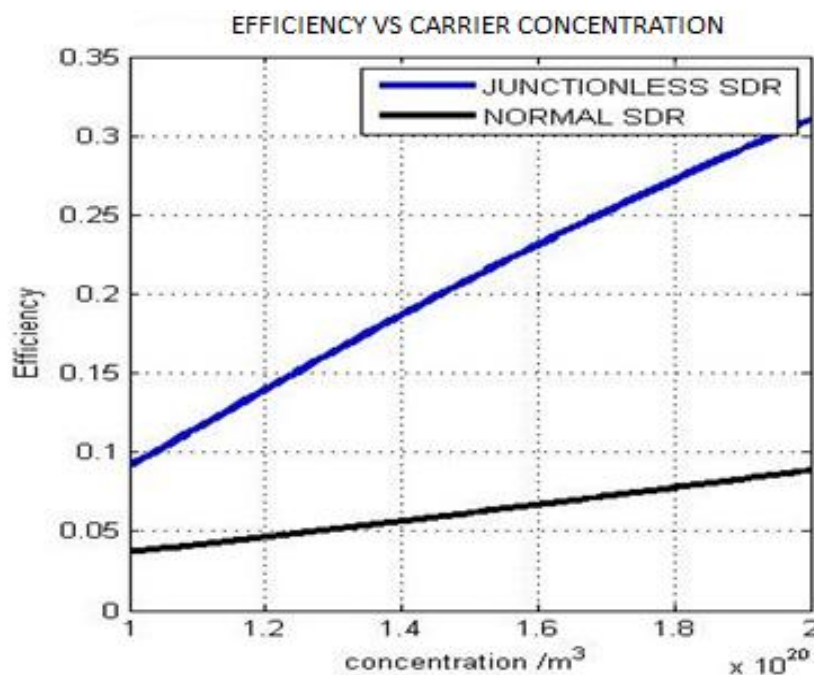
Fig.9. Variation of efficiency with the carrier concentration for a junctionless SDR IMPATT and a normal SDR IMPATT.

V. CONCLUSION

In the present work, utilizing the concept and advantages of a junctionless field effect transistor (JLTFET), an attempt has been made to present a new device structure which will function as a SDR (Single Drift Region) P+-N-N+ IMPATT diode .The analytical modeling of the electric field profile and the investigation of the efficiency of the proposed device structure have been performed based on the solution of the 2D- Poisson's equation. The proposed device structure does not require any physical metallurgical junctions and no impurity doping for creating the P+ and N+ regions. However, the voltage applied across the P+ and N+ regions can modulate the breakdown voltage and hence the efficiency can also be modulated. The electric field profile of our proposed structure resembles the electric field profile of a normal SDR IMPATT diode and without any physical doping greater efficiency can be achieved than that of a normal SDR IMPATT diode and also the efficiency can be increased by varying oxide permittivity, oxide thickness and applied voltage. However we feel it will be better if we decide the practical implementations only after fabrication and detailed characterization of these devices.

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