A Passive-Matched 22 GHz 2.6-dB-NF CMOS Front-End with a 70-800 ps Delay Block

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***Abstract*—This paper presents a power-efficient RF differential receiver front-end supporting transmitted-reference (TR) communication in a 90 nm CMOS technology. Particularly, it addresses the issues of designing the frontend amplifier with low-noise and passive matching circuits on a silicon process and integrating a low-power delay unit in the front-end with wideband characteristics. The proposed architecture includes a differential high simulated gain (11 dB) amplifier which is centered at 21.6 GHz (in the K-Band) with a 6.2 GHz bandwidth (18.1~24.3 GHz). The input and output reflection parameters have centered values around -26 and -18 dB, respectively. With noise matching, the amplifier achieves 2.6~2.9 dB bandwidth noise-figure and 2 dBm input power limit for linear coverage. To interface the amplifier with a following RF mixer, a submicron delay-block (DB) is proposed with provision of adjusting number of stages in the delay chain. The branched DB architecture achieves monotonic delays covering a range of 70-800 ps (including group-dispersion). Tweaking of delay is possible through four design parameters and the set-up is analyzed by extending the number of cascaded stages up to eight. Driven from a 1.2 V supply, the amplifier and the DB consume 13.9 and 8.52- 10.61 mW power, respectively, and realize the circuits for the TR front-end. When compared with simulated results of reported CMOS receivers, the proposed design delivers higher performance in terms of a microwave figure-of-merit.**

***Index Terms*—** CMOS Front-End, TR, Differential Amplifier, Delay-Block.

I. INTRODUCTION

In recent literature, on-chip wireless interconnects have been reported as alternatives to traditional metallic inter-chip communication which becomes possible due to scaling down of CMOS integrated circuits [1], [2], [3]. In this regard, ultra-wideband (UWB) transmission has been cited as a standard which could facilitate chip-scale wireless communication for short-distance low-power applications [4]. For intra-chip and inter-chip data transfer at submicron level, parasitic elements contributed by metallic wiring and device junctions are primarily responsible for introducing undesirable temporal dispersion within the system. This phenomenon can restrict the operating frequency of an RF font-end and limit its achievable data rate. Before transistors in a receiver circuit can move up to a spectrum above C-band (5 GHz), they have to adopt a modulation technique which can reduce these parasitic

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effects. A UWB receiver front-end with an integrated antenna can facilitate this process by moving the transmission system to a wireless domain [5]. The wideband nature of a UWB receiver can also offer additional benefits like provision to include multiple access capability and greater resistance against interference and multipath fading [6], [7], [8]. To avail these opportunities, the Federal Communications Commission has decided to allow UWB transceivers to operate in frequency ranges shared by other networks as low power density of UWB does not create interference in overlapping bands [9]. Still, proposing a satisfactory mathematical model for channel estimation remains a significant design problem for a wideband technique. The transmit-reference (TR) model, which embeds a synchronizing reference pulse within each streaming frame of data, offers a possible solution for this problem by making separate pilot-carriers redundant for receiver synchronization [10].

A typical TR receiver front-end constitutes a wideband amplifier immediately following the antenna and a self-synchronizing delay-block (DB) preceding an RF mixer [11]. As the input interfacing component of this front-end, a ~22 GHz low noise differential amplifier is presented in this paper with a 90 nm CMOS process. Supported by inductive tuning circuits, the amplifier operates between 18.1 and 24.3 GHz in the K-band which can be used for short-distance wireless transmission. The design does not require a separate current source to control its tail current and uses passive matching techniques to circumvent the need for active matching circuits at interfacing ports. The front-end forward gain (S_{21}) is 11 dB at 21.6 GHz and covers a 6.2 GHz simulated 3-dB bandwidth. While being unconditionally stable according to Rollet criterion, the amplifier dissipates ~14 mW power and may use a balun for port interfacing. In the next step, the architecture of a CMOS delay-block is portrayed which is capable of uniformly delaying wideband pulses without using bipolar power rails in the front-end. It uses basic inverter gates but employs a branched architecture to process input UWB pulses for all polarities and implement a wideband delay line necessary in a TR-receiver. Results show that, amount of pulse-delay provided by the delay-block can be regulated between 70 and 800 ps with fine tuning and low group-dispersion. The proposed integrated front-end requires ~23-24 mW power (including amplifier and DB) and suffers from low noise penalty (< 3 dB).

The paper is laid out as follows. Section II explains the architecture of a TR-receiver with emphasis on the proposed integrated front-end components. The circuits of the wideband low-NF differential amplifier and the synchronizing tunable delay-block are discussed in Sections III and IV, respectively. Section V documents the simulated figures of merit of the proposed circuits. Finally, Section VI summarizes the performance of the front-end components and compares them with examples from published literature.

II. ARCHITECTURE OF A TR TRANSCEIVER

In a transmit-reference (TR) system, the feature of self-controlled synchronization is incorporated by embedding a reference pulse in the data frame of a message signal. The reference peak facilitates

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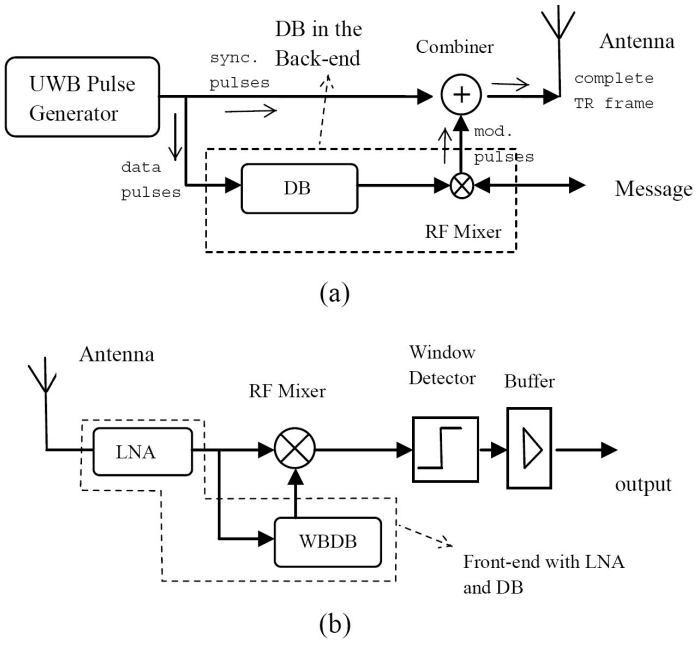

Fig. 1: a) Position of a delay-block in a transmitter employing transmit-reference b) proposed TR receiver front-end including a wideband amplifier and a delay-block.

receiver synchronization when a proper amount of delay is introduced to the received modulated signal pulses. This temporal shifting is realized with a wideband delay-block (DB) which ultimately produces a pseudo-template signal for the mixer in the receiver. A simplified model of a TR transmitter is presented in Fig. 1(a) which includes an UWB pulse generator block (PG) [10]. The reference or synchronizing (sync.) pulses generated by the PG are delivered to an RF combiner before being transferred to a transmitting antenna. The particular shape of the wideband pulses usually resembles that of a monocycle gaussian pulse. The data or message pulses (produced by the same PG) are delayed by the control mechanism of a delay-block (DB) and a radio-frequency mixer modulates them with the message signal. The RF combiner merges these modulated and reference pulses to form a frame for transmission where pulse repetition rate is regulated by the source pulse generator. So, the back-end of the TR transmitter consists of an RF combiner and a correlating RF mixer. In Fig. 1(b), the proposed TR front-end which immediately follows the receiving antenna is highlighted. It produces two responses in the form of a low noise wideband amplifier output and a delayed version of the received stream from a delay-block (generating a pseudo-pilot signal). The RF mixer in the receiver is fed with these excitations and the mixer output is processed by a window decision circuit to recover message bits encoded in the transmitted signal. Ultimately, the CMOS front-end formed with the matched amplifier and the delay-block plays a crucial role in determining noise performance and detection accuracy of a TR-receiver. This paper proposes circuit schemes to implement the proposed front-end's design blocks which will support the realization of a submicron TR-receiver.

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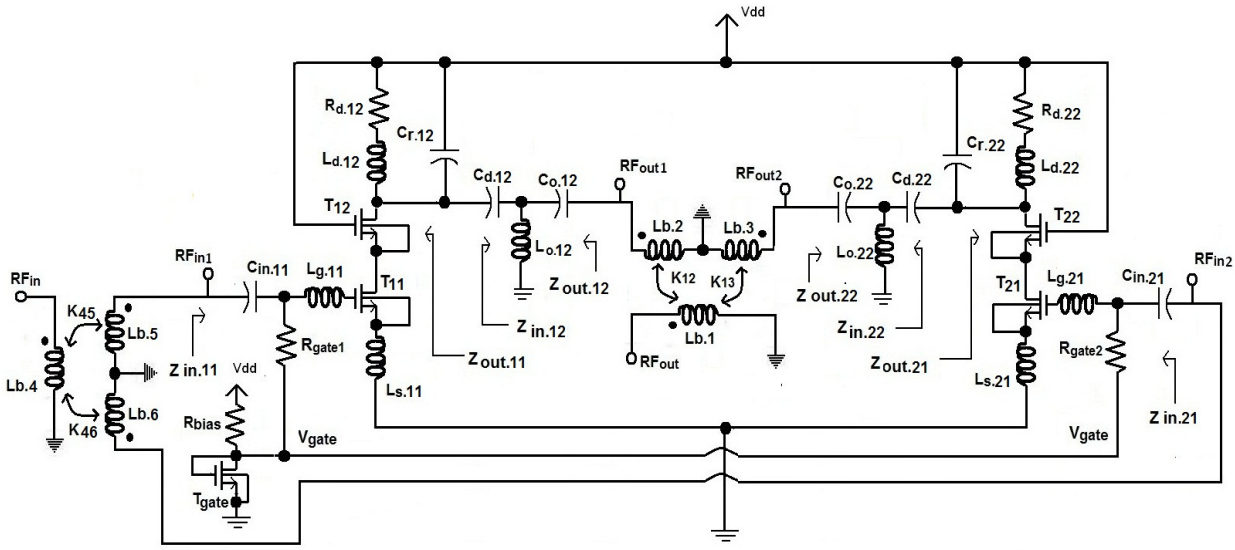

Fig. 2: The wideband differential front-end amplifier with cascode half-circuits, RF baluns, and passive matching.

III. WIDEBAND DIFFERENTIAL FRONT-END

This section focuses on the front-end in a TR-receiver which is initiated with a low noise wideband amplifier with high-gain characteristics. The proposed front-end employs a differential amplifier to avail the benefits of the differential architecture for a transmit-reference receiver circuit. It facilitates the RF mixer which is always present in the receiver to adopt a double-balanced structure (like a Gilbert mixer) and allows the circuit to be differential up to the decision section of its back-end. At the same time, this topology has to satisfy a relatively high power and area requirement. Despite this constraint, optimization of device sizes and bias currents keep the power demand for the proposed amplifier below 15 mW. As the half circuits in the amplifier core and the matching networks are symmetric in nature they make the architecture more flexible against variation of process. Other advantages include common mode noise suppression for substrate, greater reduction of power rail noise, and compatibility with dipole antenna and image rejection techniques. The differential front-end is also able to achieve a wider range of linear behavior by improving the results of the amplifier's second inter-modulation product (IP_2) [12]. The proposed amplifier architecture is presented in Fig. 2 with interfacing balanced-unbalanced (balun) circuits. In this topology made with common-source converted-to-cascode half-circuits, $L_{d.12}$ and $L_{d.22}$ resonate with the gate-drain parasites of adjoining transistors (T_{12} and T_{22}, device ratio: 50µ/0.1µ) and tuning capacitors to define the central operating frequency. The bias current through the individual half-circuits is controlled by dimension of driving devices (T_{11} and T_{21}, aspect ratio: 43µ/0.1µ) and gate biasing voltage (V_{gate}), resulting in the exclusion of a separate tail current source in series with the half-circuits. Apart from the reactance $L_{d.12}$, the resonance tank of insulating transistor T_{12} constitutes a fine-tuning parallel capacitor ($C_{r.12}$) and a small resistor ($R_{d.12}$) modeling parasitic resistance contributed by the on-chip inductor. Similarly, $C_{r.22}$ and $R_{d.22}$ are parts of the tank built on the second isolating transistor T_{22}. These insulating cascode

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devices introduce high resistance to reverse leakage and ensure isolated port operation for matching. To pre-bias the active input transistors T_{11} and T_{21}, a bias circuit is formed with the device T_{gate} (2μ/1 μ) which supplies the dc gate voltage V_{gate} (= 0.851 V) through a couple of impeding resistors ($R_{gate1/2} \approx 5\ k\Omega$). In order to match the input impedance presented by the left-half circuit to 50 in Fig. 2, a reactive LC branch ($C_{in.11}$ and $L_{g.11}$) is appended with the input gate of T_{11} along with a degenerating source element $L_{s.11}$. This branch couples the input driving signal through port RF_{in1}, reduces the magnitude of imaginary element present in input impedance, and matches the real part of port impedance to antenna resistance over centered bandwidth. $C_{in.21}$, $L_{g.21}$ and $L_{s.21}$ provide a similar service for the input device T_{21} in the right-half of this amplifier circuit. If $g_{m.x}$ is a process conductance parameter (for transistor x), $C_{gs.x}$ represents parasitic elements at the gate terminal of input transistors, and the degenerating inductor $L_{s.11}$ is connected with the source of T_{11}, input interface impedance of the amplifier without any matching can be modeled as [13]

$$Z_{inp}(with\ L_{s.11}) = \frac{g_{m.11}L_{s.11}}{C_{gs.11}} + j(\omega L_{s.11} - \frac{1}{\omega C_{gs.11}}). \tag{1}$$

After $L_{s.11}$ adjusts real element of input impedance and forward gain, equation (1) is modified with the addition of $L_{g.11}$ in the input circuit

$$Z_{inp}(with\ L_{g.11}, L_{s.11}) = \frac{g_{m.11}L_{s.11}}{C_{gs.11}} + j(\omega L_{s.11} + \omega L_{g.11} - \frac{1}{\omega C_{gs.11}}). \tag{2}$$

The final equation for input impedance matching is achieved after the LC branch is expanded with the coupling capacitor $C_{in.11}$

$$Z_{diff.left} = Z_{in.11}{}' = \frac{g_{m.11}L_{s.11}}{C_{gs.11}} + j[\omega(L_{s.11} + L_{g.11}) - \frac{1}{\omega}(\frac{1}{C_{in.11}} + \frac{1}{C_{gs.11}})]. \tag{3}$$

Input matching reduces the reactive components and modifies this expression to match it with R_{ant} which is the antenna resistance preceding the front-end amplifier. A similar expression can be derived for the right-half of the differential amplifier circuit. A balun-block will be necessary at the $RF_{in.1/2}$ ports for single to double ended signal conversion at amplifier input ports. Three coils ($L_{b.4\text{-}6}$) in a transformer formation execute this balanced to unbalanced transformation process with coupling parameters $K_{45/46}$.

Among the active devices of the amplifier, T_{11} and T_{21} are responsible for a significant share of thermal-noise. To emphasize this point, we may define a noise factor (NF_{drive}) for noise induced at gate and drain terminals of the driving transistors. The noise components for these devices are its channel noise factor (Niquist factor) , gate terminal noise coefficient , correlation factor between drain and gate noise co_{gd}, and effective quality factor of the input stage Q_{inp}. NF_{drive} also depends on amplifier center frequency (ω_o) and unity-gain transit frequency of transistors (ω_T) [14]:

$$NF_{drive} = 1 + \frac{\sigma}{\xi}[\frac{1}{Q_{inp}} - 2\left|co_{gd}\right|\sqrt{\frac{\xi^2\delta}{5\sigma}}\frac{1}{Q_{inp}} + \frac{\xi^2\delta}{5\sigma}\frac{(1+Q_{inp}{}^2)}{Q_{inp}}]\frac{\omega_o}{\omega_T}, \tag{4}$$

where ξ is defined as

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$$\xi = \frac{g_{m.11}}{g_{do.11}}, \tag{5}$$

with $g_{m.11}$ = input device transconductance and $g_{do.11}$ = zero-bias drain conductance of T_{11}. Accounting influence of driving source impedance (R_s) and gate-source inductors of input transistor, input quality factor in equation (4) can be defined as

$$Q_{inp} = \frac{\omega_o(L_{g.11} + L_{s.11})}{R_s}. \tag{6}$$

As expression of noise factor for a driving device has components accounting for drain noise, gate noise, and correlation between the two terminals and components containing in this equation have opposing polarities, they are exploited through an optimization process to reduce the noise factor. Noise components for NF_{drive} also include series resistance contributed by the inductor $L_{g.11}$ ($R_{g.11}$), gate-resistance of the input device ($R_{gate.11}$), and a process factor which is proportional to the square of input quality factor (Q_{inp}^2) [15]. Hence NF_{drive} can be expressed with another function with the form of

$$NF_{drive} = 1 + \frac{R_{g.11}}{R_s} + \frac{R_{gate.11}}{R_s} + (\frac{\sigma}{\xi}\frac{\chi}{Q_{inp}}\frac{\omega_o}{\omega_T}), where \tag{7}$$

$$\chi = 1 - 2\left|co_{gd}\right|\sqrt{\frac{\xi^2\delta}{5\sigma}} + \frac{\xi^2\delta}{5\sigma}(1 + Q_{inp}{}^2). \tag{8}$$

Typical values for these process dependent device parameters can be modeled as σ=0.667, δ=1.33, ξ=1, and co_{gd}= .39j for long channel devices and σ =2.5, δ=5, ξ=1, and co_{gd}= .4j for short channel devices [16], [17]. After canceling out the undesired elements in equation (4) with the optimization process (which keeps the power dissipation below a fixed limit), expression for minimum noise factor is simplified to two noise components (conductance ratio ξ and channel noise factor δ) apart from the operating amplifier frequencies

$$NF_{\min.p_{diss}} = 1 + 2.4\frac{\sigma}{\xi}(\frac{\omega_o}{\omega_T}). \tag{9}$$

For limited power dissipation and submicron devices, σ and δ are replaced by suitable device constants leading to

$$NF_{\min} \geq 1 + 1.62(\frac{\omega_o}{\omega_T}). \tag{10}$$

The existence of parasitic elements at the node between input and cascode devices makes noise contribution of the cascode transistor T_{12} significant, which adds on the noise factor of the overall amplifier. The sources of cascode noise factor ($NF_{cascode}$) in the proposed amplifier are the estimated parasitic capacitance associated with the intermediate node between T_{11} and T_{12} (C_{param}), zero-bias drain conductance of cascode transistor ($g_{do.12}$), secondary device transconductance ($g_{m.12}$), driving source impedance (R_s), and a bias dependent parameter (Υ_{12}) [18] which lead to

$$NF_{cascode} = 4R_s g_{do.12}\gamma_{12}(\frac{\omega_o{}^2 C_{param}}{\omega_T g_{m.12}})^2, \tag{11}$$

where C_{param} is approximated by

$$C_{param} \approx C_{gs.12} + C_{db.11} + C_{sb.12}. \tag{12}$$

Therefore, an overall noise factor of the left-half section of the amplifier circuit in Fig. 2 can be estimated by NF_{drive} and $NF_{cascode}$ and an identical factor will be applicable for T_{21} and T_{22} in the right-

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half amplifier circuit.

For the output matching circuit connected at the amplifier's left load port ($RF_{out.1}$), a design equation can be formulated for the matching components as [19]

$$Z_{in.12} = Z_{out.11}^{*} = R_{out.11} = \frac{X_{Lo.12}^{2}}{R_{load.1}}, \tag{13}$$

$$or,\ X_{Lo.12} = \sqrt{R_{out.11}R_{load.1}} = X_{Cd.12} = X_{Co.12}. \tag{14}$$

For the load-port matching circuit in the proposed design, ideally $R_{load.1} = Z_{mixer}(\Re) = 50\,\Omega$ and $R_{out.11} = Z_{out.11}(\Re) = 113\,\Omega$ in K-band (at 21.6 GHz). So, from equation (14)

$$X_{Lo.12} = 75.17\,\Omega. \tag{15}$$

A similar model equation can be obtained with $C_{o.22}$, $C_{d.22}$, and $L_{o.22}$ for the right-half amplifier circuit as

$$X_{Lo.22} = \sqrt{R_{out.21}R_{load.2}} = X_{Cd.22} = X_{Co.22}. \tag{16}$$

In this half-circuit $R_{load.2} = 50$, $R_{out.21} = Z_{out.21}(\Re) = 112\ \Omega$ near 22 GHz and consequently

$$X_{Lo.22} = 74.13\,\Omega. \tag{17}$$

As expected, the two symmetrical matching half-circuits produce similar output port impedances (at $RF_{out1/2}$) for the overall amplifier. Finally, an output balun block supports the interfacing of the amplifier with a following delay-block. To generate a direct feed for a double balanced differential Gilbert mixer, the load ports may also be linked to the mixer RF ports through small impedances. The three coils for simulating the load-port balun are designated as $L_{b.1\text{-}3}$ which are linked with carefully selected coupling constants $K_{12/13}$. In actual practice, additional fine tuning of reactive components are necessary in the amplifier circuit to obtain a sound matched response and optimize gain and noise performance.

IV. THE SYNCHRONIZING DELAY-BLOCK

As shown in Fig. 1(b), a TR-receiver can support self-synchronizing demodulation because it does not need a separate template signal for the RF correlator (mixer) in its front-end. But to realize this feature, it will require a delayed version of the received pulse-train through a wideband delay-block (DB). This delay-block should be able to handle high data rate of reference pulses and regulate them in a controlled manner. Design criteria warrant compatibility of the delay-block with different amplifier topologies as it is placed between a low noise amplifier and a radio-frequency mixer in the receiver chain. Usage of variable delay units have been reported in applications ranging from voltage controlled oscillators (VCO) to pulse width control systems (PWCL) [20]. But a wideband delay-block for a TR-receiver demands special focus on minimizing power dissipation as the system needs to keep the average power density to the lowest permissible level [21]. Moreover, these delay elements require wideband characteristics to be able to handle pulses with a duration of 10^{-10} s.

The proposed architecture of a divided wideband delay-block (DB) built with 90 nm transistors and capable of processing bipolar message carrying pulses [22] is presented in Fig. 3. At its input port, the delay-block has an optional three-coil signal conversion block (L_{b7}, L_{b8}, and L_{b9}) to generate separate

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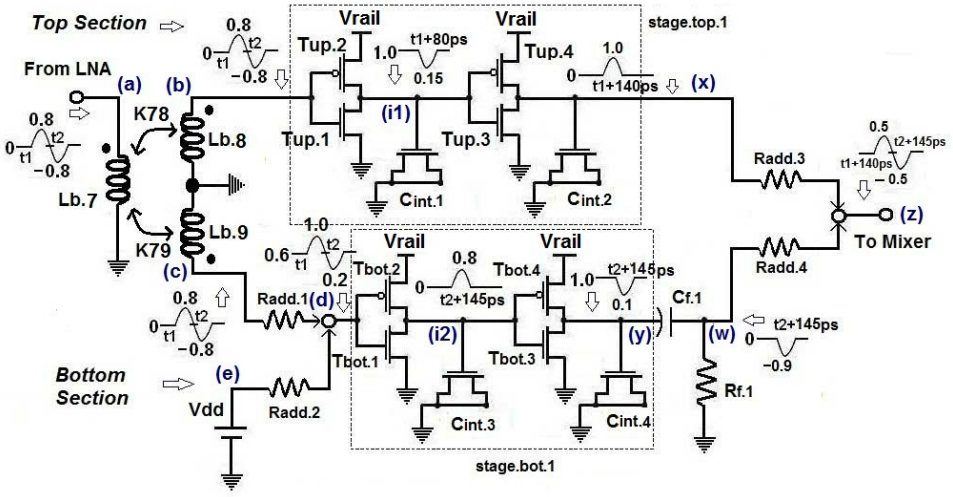

Fig. 3: The proposed single-stage delay-block (DB) with two parallel branches.

excitations for its top and bottom branches (at nodes *b* and *c*). No loss in strength of the input feed is assumed in the conversion process (ideal coupling). The bottom feed is added with a bias voltage (V_{dd}=1.2 V) through a resistive summer to generate an elevated pulse train (at node *d*). To drive the delay-block and verify its delay regulation, an 800 mV test signal is applied to the proposed architecture. The strength of these test pulses can be tuned by adjusting the gain granted by the preceding amplifier. The primary objective of using two parallel sections in the circuit is to ensure uniform delay for all member pulses in the driving stream and power the delay block with a single bias rail (V_{rail}). For a single-stage DB, as shown in Fig. 3, the sectional delay chains ($stage_{top.1}$ and $stage_{bot.1}$) are built with a pair of cascaded inverter blocks and two intermediate capacitors. The unit $stage_{top.1}$ is formed with devices $T_{up.1}$ (14µ/0.1µ), $T_{up.3}$ (1µ/0.1µ), $T_{up.2/4}$ (16 µ/0.1µ) and drain-source shorted transistors contributing junction capacitance ($C_{int.1=2}$, in the range of 100 fF). The driving stream for the bottom unit ($stage_{bot.1}$) has a base voltage offset of 0.6 V and a different peak-to-peak coverage. As a result, it uses transistors with adjusted dimensions {$T_{bot.1}$ (20µ/0.1µ), $T_{bot.3}$ (8µ/0.1µ), $T_{bot.2/4}$ (16 /0.1)} and 50 fF shunt capacitors ($C_{int.3/4}$). Output from these parallel units (at points *x* and *y*) produces nearly uniform delays for bipolar pulses (average of 180 ps for a single block). In order to process negative pulses, the driving stream base was elevated to the 0.6 V range at the start of the bottom unit. As a result, a dc component of 1.0 V is present in the delayed signal at node *y* of $stage_{bot.1}$. This element is removed by an RC branch (made of $R_{f.1}$ and $C_{f.1}$) and the pulse base is brought back to near ground level. $R_{add.3}$ and $R_{add.4}$ form a second resistive summer which combines the sectional responses to generate a complete delayed pulse train at node *z* with relatively small signal dispersion. The overall delay achieved by the proposed single-stage DB is not fixated at 180 ps but can be fine tuned with a number of design parameters [22], as will be explained in the following sections.

The branched architecture of the delay-block allows extension of number of stages in each section (up to eight) during the testing process. Fig. 4 presents a four-stage wideband delay-block where eight delay units ($stage_{top.1-4}$ and $stage_{bot.1-4}$) are divided between two sections/branches of the

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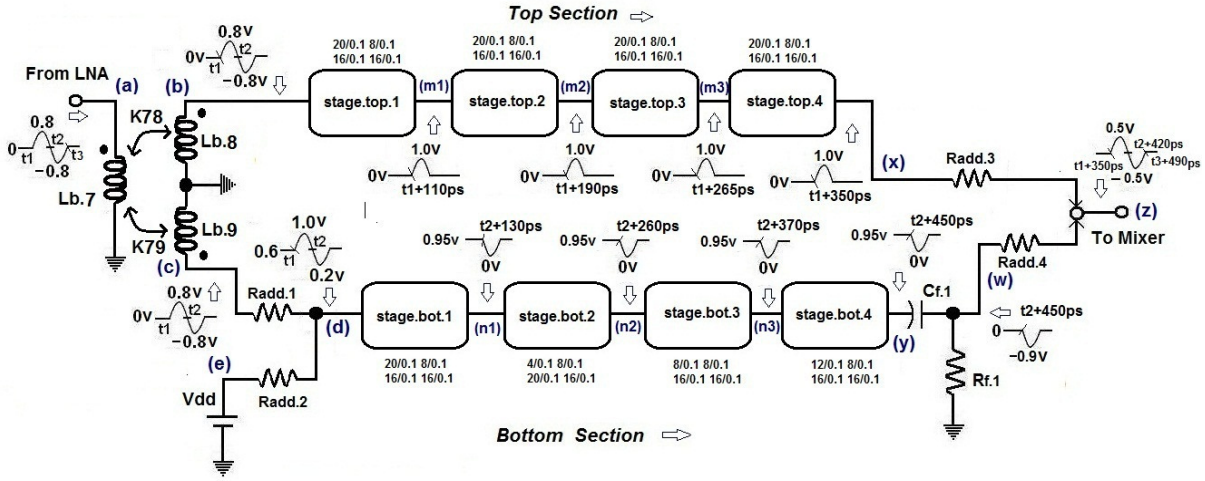

Fig. 4: A complete four-stage delay block (extendable to eight stages).

design. The device sizes (mentioned in the figure) remain consistent for the top section but need to be adjusted to deal with base elevated pulses in the bottom section. The progress of the delayed pulses at the intermediate nodes (m_i and n_j with $\{i, j\}$=1-4) is shown in the diagram which indicates a regular and monotonic variation of achieved delay. The four-stage DB introduces an average overall delay of ~420 ps and the difference in temporal positions of the negative pulse (t_2+450 ps at node *w* and t_2+420 ps at point *z*) can be attributed to the resistive summation process. By controlling gain provided by the amplifier preceding the delay-block, the strength of input pulses and magnitude of dc offset needed in the bottom section can be predesigned. Since the wideband pulses are essentially regenerated in this scheme, no matching circuit will be needed for the delay-block as in the cases of LNA and RF mixer in the receiver chain. Further discussion on tuning and regulation of the proposed delay-block is documented in the result section.

The expression for propagation delay achieved by the complete delay chain indicates a non-linear relationship between overall delay and number of stages or individual delay units in top and bottom sections. The pair of cascaded inverters in a single-stage branch, as shown in Fig. 3, controls the component delay with rail voltage (V_{rail}), shunt reactance (C_{int}), and device dimensions (W/L ratio) working as design parameters. For a single inverter gate, the value of saturation current flowing through the transistors ($I_{saturation}$) is considered as average bias tree current and approximated by

$$I_{bias} = I_{saturation} = \frac{G_n}{2}(V_{gs} - V_{th,n})^2, \tag{18}$$

where the device (pull-down) threshold level is designated as $V_{th.n}$ and G_n is transistor transconductance gain. A mirror equation obtained for the pull-up device will produce the same magnitude for the bias current. If strength of input pulses and voltage of bias rail are regulated in the circuit then the following relationship can also be maintained

$$V_{gs} \approx V_{rail}. \tag{19}$$

After we define $t_{del.high.low}$ and $t_{del.low.high}$ as propagation delays for the signal during high-to-low or low-to-high transition at inverter output and C_{shunt} as intermediate shunt capacitance, unit inverter-delay for a delay gate can be derived as [23]

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$$t_{del.inv} = \frac{1}{2}(t_{del.high.low} + t_{del.low.high}). \tag{20}$$

If $R_{eq.p}$ and $R_{eq.n}$ represent equivalent resistances when pull-up and pull-down transistors are 'on', FET signal transition times will be proportional to time constant of RC networks formed by device (which is on) resistance and shunt (load) capacitors. When signal drops from high to low at inverter output, the reactive network is realized with $R_{eq.n}$ and output capacitance C_{shunt}. On the other hand, $R_{eq.p}$ becomes part of this RC circuit in case of low to high transition at gate output. Therefore, propagation delays can be defined with the functions

$$t_{del.high.low} = (\ln 2)\,R_{eq.n}\,C_{shunt}, \tag{21}$$

$$t_{del.low.high} = (\ln 2)\,R_{eq.p}\,C_{shunt}. \tag{22}$$

Using these definitions and expressing 'on' resistance in terms of transistor sizes lead to [23]

$$t_{del.inv} = \frac{(\ln 2)C_{shunt}}{2}(R_{eq.p} + R_{eq.n}) \tag{23}$$

$$\approx \frac{C_{shunt}}{2V_{rail}}\left(\frac{1}{G_p} + \frac{1}{G_n}\right) \tag{24}$$

$$= \frac{C_{shunt}}{2V_{rail}C_{ox}}\left(\frac{L_p}{\mu_p W_p} + \frac{L_n}{\mu_n W_n}\right), \tag{25}$$

where C_{ox} is unit capacitance of silica layer, $\mu_{p/n}$ is mobility of carriers, and $(W/L)_{p/n}$ denotes sizes of concerned transistors. Derivation of equation (32) assumes an insignificant transition time for the driving signal at the input of the delay-block. In contrast, wideband pulses spend a finite amount of time to rise or fall at the input node and after this transition time is designated as $t_{up/down}$, corresponding delay equations at the output port will be modified as

$$(t_{del.high.low})^* = \sqrt{(t_{del.high.low})^2 + (t_{up}/2)^2}, \tag{26}$$

$$(t_{del.low.high})^* = \sqrt{(t_{del.low.high})^2 + (t_{down}/2)^2}. \tag{27}$$

Therefore, the final expression of inverter-delay for an individual gate will take the form of

$$t^o_{del.1.stage} = \frac{1}{2}[(t_{del.high.low})^* + (t_{del.low.high})^*]. \tag{28}$$

If C_{shunt} accounts for only design values of intermediate capacitors, external loading capacitance from a following RF component is modeled as C_{extra}, input gate capacitance of the delay-block is defined with C_{gate}, and equation (28) is modified as

$$t_{del.1.stage} = t^o_{del.1.stage}\left(1 + \frac{C_{extra}}{\gamma C_{gate}}\right), \tag{29}$$

where γ (≈ 1 for a 90 nm process) is a process-dependent proportionality factor. For an M-inverter N($=\frac{M}{2}$)-stage delay-block branch, the final expression will look like [23]

$$t_{del.N.stage} = (2N)t^o_{del.1.stage}\left[1 + \frac{(F)^{\frac{1}{2N}}}{\gamma}\right], \tag{30}$$

where F is overall effective fan-out of the delay unit. The power penalty suffered by a CMOS delay-

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block is expected to have three major components [24]. They include a dynamically dissipated power element ($P_{dynamic}$) arising from movement of charge through the shunt capacitor C_{shunt} at a switching frequency of f_{op}, a short-circuit power (P_{sc}) component consumed when both transistors in an inverter gate are on simultaneously with a peak current I_{max} and conduction duration t_{on}, and a static power (P_{static}) element dissipated by reverse leakage current $I_{rev.leak}$. The overall power figure for a complete wideband delay-block will depend on number of stages used in the delay chain sections, optimized rail voltage, intermediate capacitance, and finger width of devices. After being processed by the delay-block, the received signal will leave the front-end and be fed to the following radio-frequency mixer in the TR-receiver.

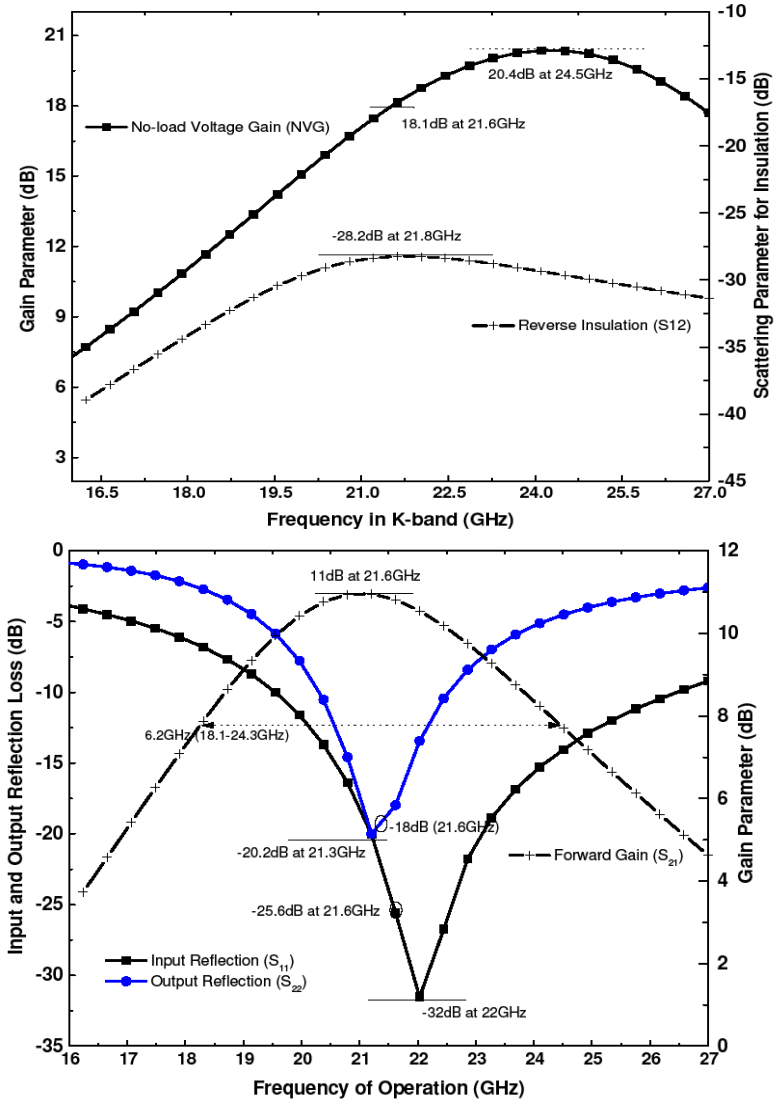

Fig. 5: a) No-load voltage gain and reverse isolation of the front-end around K-band b) forward gain (S21) and port reflection (S11 & S22) parameters.

V. RESULTS AND DISCUSSION

The proposed receiver blocks are designed with an RF simulator including layout parasites generated by 90 nm circuit components to facilitate accurate RF analysis.

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A. Wideband Differential Front-end

As the first section of the proposed TR-receiver front-end, the design parameters of the differential wideband low noise amplifier are analyzed with the CMOS process. The 90 nm amplifier is able to achieve high small signal gain and keep noise ceiling and power penalty below 3 dB and 15 mW, respectively. During parameter extraction, the LNA is interfaced with balun-circuits and a matched 50 load.

1) *Forward Gain and Port-Reflection Parameters:* The peak voltage gain (PVG) of the differential low noise amplifier with an open-circuited load-port is 20.4 dB in the K-band (24.5 GHz) and 18.1 dB at the center frequency (21.6 GHz), as shown in Fig. 5(a). It also shows that resistance to reverse isolation (S_{12}) is always greater than 28.3 dB and can reach up to 35 dB within the message bandwidth. In Fig. 5(b), maximum forward gain (indicated by S_{21}) is 11 dB, peaking at 21.6 GHz and presenting a 3-dB-bandwidth of 6.2 GHz (18.1-24.3 GHz). The same frame plots input and output port matching parameters (S_{11} & S_{22}) with minima at -32 dB and -20.2 dB, respectively, in the 21-22 GHz range. The port return loss at the amplifier peak frequency (21.6 GHz) are -25.6 dB and -18 dB, in that order. Therefore, undesirable port-reflection remains insignificant over the concerned frequencies for the amplifier.

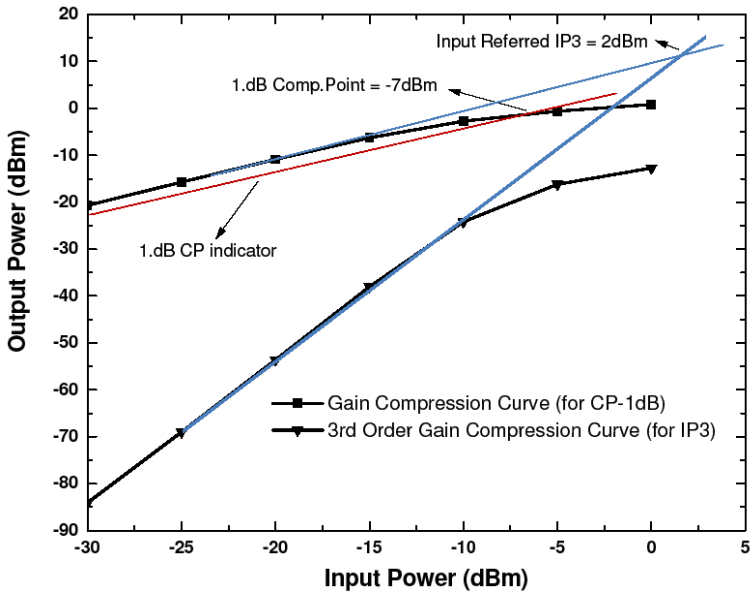

Fig. 6: Linear range of amplifier operation as manifested by input-port referred 1dB-CP and IP_3.

2) *Estimation of Linear Behavior from the Amplifier:* As the power of its driving signal (in dB_m) is raised for the wideband amplifier, the input-referred one-decibel compression point (1dB-CP) is eventually crossed at -7.24 dB_m and the projection modeling the third-order intercept point (IIP_3) intersects the input power axis at 2 dB_m before the amplifier enters a non-linear region of gain compression (see Fig. 6). At the compression point the amplifier is expected to deliver 2 dB_m power to a matched load while still remaining in linear domain and the estimated output power at IIP_3 point is 12 dB_m.

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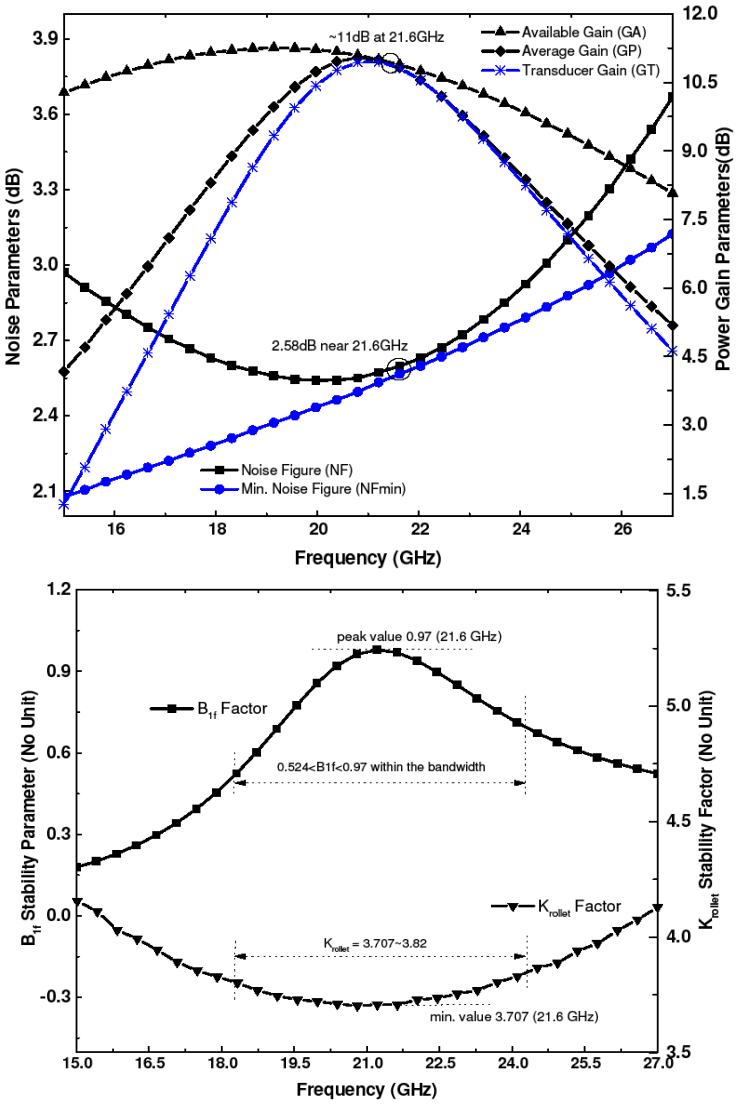

Fig. 7: a) Noise parameters and B1f factor (for amplifier bandwidth) b) power gains provided by amplifier core and matched amplifier accompanied with Rollett (Krollet) factor.

3) *Noise:* With the employment of a differential topology, the designed front-end is able to maintain its noise parameters below the ceiling of 3 dB (2.58-2.97 dB). Its projected noise figures (NF and theoretical NF_{min}) are documented in Fig. 7(a) which coincide around the center point. NF settles around 2.58 dB near the center frequency (21.6 GHz) and approaches a minimum peak of 2.5 dB at the edge of its bandwidth, indicating optimum noise performance over this frequency coverage.

4) *Power Gain and Power Penalty:* Among an amplifier's power gain parameters, available gain (GA) provides an estimation of power gain provided by the core amplifier which is lowered down to transducer gain (GT) after the addition of port-matching networks. In Fig. 7(a), GA, GT, and GP (average power gain) coincide near 11 dB around the center frequency which can be interpreted as an indication of successful port-matching. Maintaining its compatibility with low power on-chip transceivers, dc power consumed by the font-end is measured as 13.9 mW when amplifier half-circuits and bias circuitry are powered with 5.72 and 0.2 mA currents, respectively.

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5) *Estimation of Stability (K_f and B_{1f} factors):* The amplifier is expected to be behave in an unconditionally stable manner over all frequencies around the message bandwidth. To assess this quality, the microwave stability factor B_{1f} is defined in terms of scattering parameters

$$B_{1f} = 1 + \left|S_{11}\right|^2 - \left|S_{22}\right|^2 - \left|\Delta\right|^2, \tag{31}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}, \tag{32}$$

which is required to satisfy the following condition

$$B_{1f} > 0 \; over \; the \; bandwidth. \tag{33}$$

When presented in Fig. 7(b), B_{1f} is found to have a magnitude between 0.524 and 0.97 in the concerned range of bandwidth (18.1-24.3 GHz). To verify this result with a second stability parameter, the Rollett stability factor (K_{rollet}) is also plotted in the same figure with its value always being greater than a unit limit (fulfilling its criterion of stability) [13]. This factor is also defined with s-parameters

$$K_{rollet} = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{21}\right|\left|S_{12}\right|} \tag{34}$$

and has a relatively flat profile (3.71-3.82) with a lowest trough of 3.707 at 21.6 GHz. As a result, the amplifier will provide resistance to oscillation induced by white noise which may get accumulated in the circuit during its start-up mechanism.

B. Wideband Delay-Block (DB)

The proposed wideband delay-block (DB) to follow the front-end amplifier is also built with 90 nm CMOS devices as a part of the TR-receiver architecture. To illustrate the progression of a driving bipolar pulse stream through a multi-stage delay chain, a six-stage delay-block (built with the same principle presented in Fig. 4) is subjected to a pulse train of monocycle gaussian pulses. Fig. 8(a) presents the time domain signals existing at different nodes of the top section for a complete six-stage DB. Delayed versions (130-500 ps) of the positive half of the input pulse are collected from output nodes (m_1-m_6) of six successive stages (See Fig. 4) and a sample intermediate node (i_1) in the first stage of the delay chain. A symmetric balun produces identical replicas of the the driving pulse and feed them as sectional inputs (at points b and c). In Fig. 8(b), after the input pulse is elevated with a bias voltage (V_{dd}) for the bottom section, the driving signal is now collected from point d. Delayed versions for the elevated negative-half of the input signal show a progression of 150-650 ps at output nodes of stages in the bottom section (n_1-n_6). The final response (at node *y*) gathered after six stages in the bottom section is decoupled (dc component removed) at node w as shown in Fig. 8(c). It also shows the signal produced by the output combiner (culminating at node *z*) which manifests an average delay of 620 ps. Similar number of stages are employed in the DB branches to achieve identical and uniform delay for all pulse elements. The responses demonstrate that monotonic and quasi-linear rise in delay is available at output node of each of the six stages. To measure this phenomenon,

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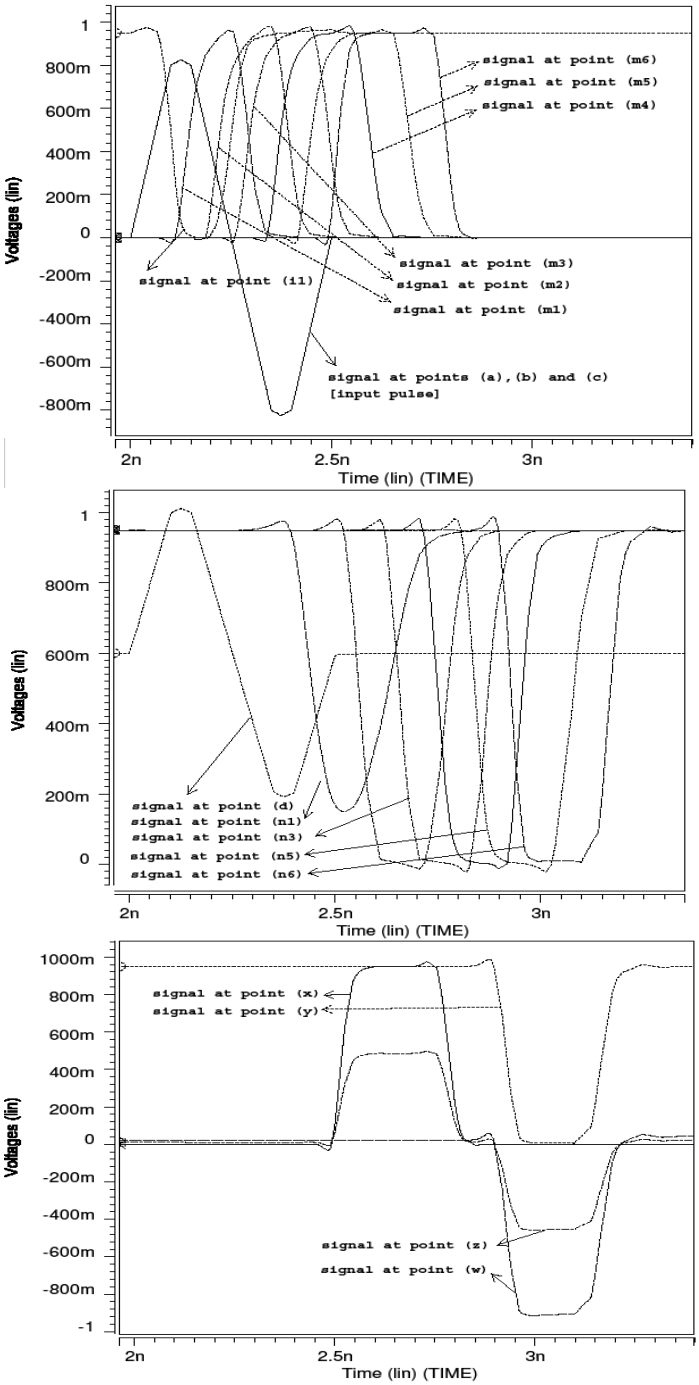

Fig. 8: Progression of delayed response as achieved through a six-stage delay-block at different points a) for top section b) for bottom branch c) overall response.

$(W/L)_{p.(up/bot).q}$ is selected as the notation to define dimension of individual transistors and $C_{p.int.q}$ expresses value of a shunt DB capacitor where *p=1-6* are stage indices of delay sections and *q=1-4* indicate individual transistors or capacitors for a particular stage. To produce the response in Fig. 8, V_{rail} is set to 0.95 V and dimensions of the first stage are selected as

$$(\frac{W}{L})1.up.1 = \frac{14}{0.1}, (\frac{W}{L})1.up.3 = \frac{1}{0.1}, \tag{35}$$

$$(\frac{W}{L})1.bot.1 = \frac{20}{0.1}, (\frac{W}{L})1.bot.3 = \frac{8}{0.1}, \tag{36}$$

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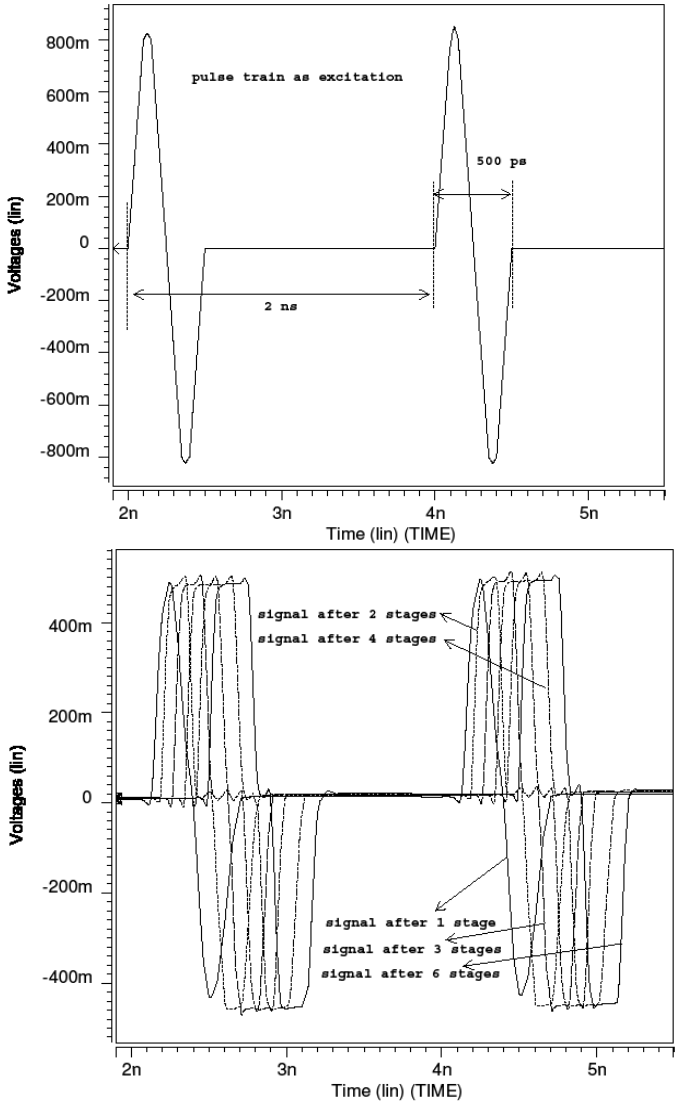

Fig. 9: a) Input wideband pulse stream of monocycle gaussian pulses b) delayed versions at the final output port of the delay-block while varying the number of stages.

$$(\frac{W}{L})1.up.2 = (\frac{W}{L})1.up.4 = (\frac{W}{L})1.bot.2 = (\frac{W}{L})1.bot.4 = \frac{16}{0.1}. \quad (37)$$

The other five stages require manipulation of device dimensions to compensate for any signal drop at intermediate nodes. Power dissipated by a single-stage delay-block is kept below 9 mW and for a six-stage delay unit power penalty reaches up to 10.6 mW. According to design requirement, number of stages in the DB can be varied to achieve regulated temporal shifts. The signal typically collected by a TR-receiver front-end is shown in Fig. 9(a) in the form of a wideband pulse stream made with monocycle gaussian pulses. Fig. 9(b) presents its delayed versions collected from the output ports of the proposed multi-stage delay-block. In addition to the number of stages in a DB section, tuning of delay may also be controlled by shunt capacitors, ratio of transistors, and magnitude of rail voltage [22]. This phenomenon is further illustrated in tabular form for a single-stage delay-block in the following section.

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TABLE I

RELATIVE PERFORMANCE OF THE PROPOSED 90 NM FRONT-END AMPLIFIER

Reference	This Work	[25]	[26]	[27]	[28]
Operating Point (GHz)	21.6	23.5	5.0	3.0	7.0*
Amount of Noise (dB)	2.61	4.5*	3.8	4.0	–
IIP3 (dBm)	2	-3	2	4	8.5
Power Penalty (mW)	13.97	24	7	9	23
Process (CMOS)	.09μm	.13μm	.18μm	.18μm	.18μm
No of Stages	1	2	–	–	1
Small-Signal Gain (S_{21}, dB)	11	20	10	9.7	13.2*
Message Bandwidth (GHz)	6.2	5.2	7.4	7.5	–
Min. Port-Reflection (S_{11}, dB)	-31.9	-9	–	–	–
Min. Port-Reflection (S_{22}, dB)	-20.2	-14	–	–	–
Peak Insulation (S_{12}, dB)	-28.2	–	–	–	–
Topology	Differential	Differential	Distributed	Distributed	Feedback
FOM (eq. 47)	10.56	5.59	2.55	1.08	–

* Estimated simulated results

VI. SUMMARY OF PERFORMANCE

A. Front-End Amplifier

The synopsis of simulated performance extracted from the proposed differential front-end is summarized in Tables I and II where it is compared with simulated results of published wideband amplifier circuits [25]-[32]. To enable relative evaluation of amplifiers built on different scales of CMOS technology, a composite FOM (figure-of-merit) parameter is defined as

$$FOM = \frac{S_{21}(dB)\, Center\ Freq.(GHz)}{Power(mW)\ \{NF_{\min}(dB) - 1\}}. \tag{38}$$

In summary, the proposed amplifier achieves a better figure of merit (10.5) and realizes a 22 GHz TR front-end customized for low-NF (2.6 dB) high-gain (11 dB) moderate power (13.9 mW) applications.

B. Delay-Block

The literature on the proposed delay-block has estimated that tuning of shunt capacitors and transistor dimensions will raise the group-delay achieved by the chain and increasing the rail voltage will have an opposite effect. To verify these predictions, performance of a single-stage delay-block under regulation is summarized in Table III where its specified controlling parameters (including number of cascaded stages) are varied. Among the four shunt capacitors of a single-stage DB, $C_{1.int.1}$ provides fine tuning (range of 50 ps) while other reactances are set to fixed values ($C_{1.int.3}$=$C_{1.int.1}$ and $C_{1.int.4}$=$C_{1.int.2}$=50 fF). Progression of bipolar peaks through the delay-block becomes non-uniform when device dimension is varied as their negative peak suffers from higher group dispersion. In Table III, $W_{1.up.1}$ and $L_{1.up.1}$ are manipulated as control figures for a delay variation of 150 ps when $W_{1.up.3}$=8 µm and $W_{1.up.2}$=$W_{1.up.4}$=16 µm. The third control parameter of the DB (rail voltage, V_{rail}) achieves a range of delay regulation which is nearly 200 ps. With total number of stages varying between one and eight, range of coarse adjustment for overall delay is measured as 180-790 ps. Power requirement

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TABLE II

RELATIVE PERFORMANCE OF THE PROPOSED 90 NM AMPLIFIER (CONTD.)

Reference	[29]	[30]	[31]	[31]	[32]
Operating Point (GHz)	20.5	5	8	2	1
Amount of Noise (dB)	4.1	2.8	3.9	1.8	1.8*
IIP3 (dBm)	10	1	-7	-8	-2.2
Power Penalty (mW)	46	14	20	24	3.6
Process (CMOS)	.25μm[b]	.065μm	.09μm	.09μm	.18μm
No of Stages	1	1	2	2	2
Small-Signal Gain (S_{21}, dB)	10.3*	5.3	9	17	25*
Topology	SIDO[a]	Differential	Differential	Differential	Differential
FOM (eq. 47)	1.48	1.05	0.93	1.77	8.68

* Estimated simulated results

[a] Single In Differential Out

[b] SiGe Process

TABLE III

TUNING PERFORMANCE OF THE 90 NM PROPOSED DELAY BLOCK IN FIG. 4

Effect of shunt capacitors on a single-stage DB			Delay of a single-stage DB against varying device dimension			Delay for a single-stage DB with varying rail voltage		Delay achieved with multiple stages in the delay-block		
$C_{1.int.1}$ (fF)	$C_{1.int.2}$ (fF)	Delay (ps)	Param.1 (μm)	Param.2 (μm)	Delay (ps)	Rail Vol. (V)	Delay (ps)	No. of Stages	Delay (ps)	Peak Power (mW)
30	50	130	$W_{1.up.1}$=8	$L_{1.up.1}$=0.1	340	.8	250	1	180	1.52
40	50	140	$W_{1.up.1}$=16	$L_{1.up.1}$=0.1	230	.90	180	2	258	1.995
50	50	150	$W_{1.up.1}$=20	$L_{1.up.1}$=0.1	200	0.95	150	3	343	2.76
60	50	150	$W_{1.up.1}$=30	$L_{1.up.1}$=0.1	170	1.0	130	4	420	3.04
70	50	160	$W_{1.up.1}$=40	$L_{1.up.1}$=0.1	140	1.05	110	5	523	3.306
80	50	160	$W_{1.up.1}$=40	$L_{1.up.1}$=0.14	170	1.1	100	6	620	3.449
90	50	170	$W_{1.up.1}$=40	$L_{1.up.1}$=0.16	180	1.15	90	7	700	3.563
100	50	180	$W_{1.up.1}$=40	$L_{1.up.1}$=0.2	190	1.2	70	8	790	3.61

for the delay-block has a fixed component (7 mW) for summer circuits and the remaining power element (peak) varies between 1.5 and 3.6 mW as eight stages are cascaded in both sections of the delay chain.

VII. CONCLUSIONS

This paper proposes circuit-level implementation of a 22 GHz 90 nm CMOS receiver front-end suitable for the principle of transmitted-reference (TR) communication. Using an LC port-matching technique, the front-end amplifier realizes a differential topology with high simulated gain (11 dB) to improve system noise performance (below 3 dB). Base NF ceiling for the wideband amplifier is expected to be 2.6 dB and the circuit consumes 13.9 mW when driven from a 1.2 V bias rail. Over its 6.2 GHz bandwidth, reverse isolation for the front-end is better than the margin of -28 dB with minimum port-matching parameters of -32 dB and -20.2 dB, respectively. A wideband 90 nm delay-block (DB) completes the CMOS front-end which is capable of producing a delayed version of the received pulse train. The dynamic DB circuit sections are extendable to eight stages and monotonic

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regulation of bipolar delay in the range of 70-800 ps is attained with four control parameters. Comparison with simulated reported designs establishes a superior figure-of-merit for the front-end amplifier and along with the delay-block it would complement the realization of a TR transceiver in circuit level.

VIII. ACKNOWLEDGMENT

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